5291 ppi OLED Display with C-Axis Aligned Crystalline Oxide Semiconductor

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ABSTRACT

C-axis aligned crystalline oxide semiconductor field-effect transistor (CAAC-OS FET) can be scaled down to a width and length of 60 nm. We have fabricated an organic light-emitting diode (OLED) display with more than 5000 ppi required in virtual reality (VR) displays by using CAAC-OS FETs as the backplane.

1 INTRODUCTION

Virtual reality (VR) technologies have recently been gaining a lot of attention [1–3]. One of the requirements for the development of more realistic VR worlds is the fabrication of displays with higher resolutions [4–6]. For example, head-mounted displays (HMDs) used for VR require displays with more than 5000 ppi to prevent users from noticing the pixels when looking at them from a short distance. Recently developed small, medium, and large displays utilize field-effect transistors (FETs) the size of a few micrometers, but the fabrication of a high-resolution display with more than 5000 ppi would require the use of FETs smaller than a micrometer within the pixels. However, scaled down FETs may negatively affect the display performance due to phenomena such as the short channel effect.

Oxide semiconductors (OS) of indium gallium zinc oxide (IGZO) were first synthesized by Kimizuka et al. in 1985 and have been widely researched since [7–10]. Yamazaki et al. proposed a c-axis aligned crystalline IGZO (CAAC-IGZO) [11], and it is neither crystal nor amorphous but “an intermediate state” between crystal and amorphous states [12]. FETs that employ CAAC-IGZO in their active layers (CAAC-OS FETs) exhibit features that are not observed in Si-FETs, such as an extremely low off-state current and a high on–off ratio [13-15]. They also have the advantage of not requiring a laser crystallization process, which has recently made CAAC-IGZO widely used as an alternative to low-temperature polycrystalline silicon (LTPS) and hydrogenated amorphous silicon (a-Si:H) backplanes [16, 17]. Furthermore, CAAC-OS FETs are less likely to suffer from a short channel effect than Si-FETs, hence they also exhibit an advantage in terms of scaling [18]. Owing to this feature, applications to memory and LSI are being evaluated for CAAC-OS FETs [19, 20].

In this paper, we propose a high-resolution organic light-emitting diode (OLED) display with more than 5000 ppi that utilizes CAAC-OS FETs with a width and length of 60 nm as the backplane.

2 MOTIVATIONS

2.1 Displays with a Pixel Density of 5000 ppi

In one type of VR applications, users wear an HMD and images are projected through a display mounted in the headset. Hence, wearable displays in the form of goggles and glasses are being developed as HMDs. If lenses are not being used, the distance between the HMD display and the eyes of the person wearing the headset is between 12 mm and 40 mm. According to the calculation completed by R. N. Clark, the visual acuity of the human eye is 0.59 arcminutes per line pair [21]. Based on this visual acuity and assuming that the distance between the eyes and the display is 30 mm, headset wearers would not be able to notice each pixel in front of their eyes if the pixel pitch is approximately 5.15 μm. This pixel pitch corresponds to a display resolution of approximately 5000 ppi. Therefore, the projection of realistic VR images in an HMD would be enabled by incorporating a high-resolution display with more than 5000 ppi.

2.2 Properties of CAAC-OS FET

The display resolution used in smartphones is between 400 ppi and 500 ppi, whereas VR requires displays with more than 5000 ppi. In other words, the size of each sub-pixel of a realistic VR display would be approximately 3 μm, meaning the transistors used in devices similar to smartphones are too large and unsuitable for VR displays. Moreover, the amount of electric current that flows in each pixel of OLED displays is proportional to the pixel size, hence the amount of electric current that flows through the device would be smaller. Consequently, backplanes for displays with more than 5000 ppi would require the following properties:

i) Transistors with short channel length.

ii) Current capability suitable for controlling an OLED device.

For this reason, we adopted CAAC-OS FETs for the backplane. Figure 1 (a) shows a perspective view of CAAC-OS FET. Figure 1 (b) and Figure 1 (c) show the cross-sectional view of CAAC-OS FET in the A-A’ direction (channel length direction) and B-B’ direction (channel width direction) respectively. As presented in Figure 2 (a), a CAAC-OS FET exhibits favorable Id-Vg characteristics even though its width (W) and length (L) are equal to 60 nm (W/L = 60 nm/60 nm). Figure 2 (b) shows the FET’s gate breakdown voltage. The gate leakage is virtually negligible up to 10 V.

As Si and LTPS FETs have a large current capability, when they are used as OLED driving transistors, their length and saturation are increased and their current capability is limited. Furthermore, when their length is increased, their layout area also increases, meaning they

cannot be arranged suitably to meet the amount of current required for high pixel density OLED displays, and this affects what is displayed. In contrast, CAAC-OS FETs exhibit favorable saturation characteristics even when their length is short and a suitable amount of current flows to control OLED devices. Hence, CAAC-OS FETs are suitable for backplanes of high-resolution OLED displays.

An additional feature of CAAC-OS FET is its extremely low off-state current. As shown in Figure 2 (a), the off-state current is smaller than 1 x 10^{-12} A, which is below the measurement limit. Therefore, when the display shows black, the amount of electric current that flows would be extremely small, leading to a low power consumption.

3 RESULTS

3.1 Circuit Configuration and Operation

Figure 3 (a) shows a block diagram of a scan driver, and Figure 3 (b) shows one of the shift registers composing the scan driver. The proposed scan driver is configured with shift registers connected in series. A start pulse is input into the first-stage shift register, and with four-layer CLK and PWC, the first-stage shift register generates a shift pulse and a gate signal for the next-stage shift register.

The method in which shift pulse and gate signal are generated from SROUT and GOUT respectively is described using Figure 3 (b).

First, node O1 and node O2 are initialized to GVSS and GVDD-Vth (Vth corresponds to the threshold voltage of the CAAC-OS FET) respectively. At this point, GOUT and SROUT are both fixed as GVSS.

Then the shift pulse of SROUT in the previous stage is input to LIN, changing the voltage of node O1 and node O2 to GVDD-Vth and GVSS respectively. The voltage of node O1, GVDD-Vth, is input to node OA via M5, and to node OB via M8. As a result, M6 and M9 are turned on. The voltage of node O2, GVSS, is input to the gates of M7 and M10, turning them off.

With M6 and M9 turned on as described above, the voltages of GOUT and SROUT increase when CLK1 and PWC1 are changed from LOW to HIGH voltage. With this, bootstrap capacitors C2 and C3 increase the gate voltages of M6 and M9 from GVDD-Vth. Thus, the shift pulse and the gate signal are output from SROUT and GOUT respectively, without the signal being attenuated by Vth. In this case M5 and M8 contribute to efficiently increasing the gate voltages of M6 and M9.

3.2 Pixel Structure

Figure 4 shows a sub-pixel circuit diagram of our display prototype using an OLED device. The configuration of each pixel is 2Tr1C. In all the sub-pixels, the selection FET M1 is an OS-FET with W/L = 60 nm/60 nm, and the driving FET M2 is an OS-FET with W/L = 60 nm/200 nm. The symbol C1 represents a storage capacitor.

As the display prototype is of a high pixel density, the pixels are arranged in a zigzag pattern similar to that in [22]. The sub-pixel pitch is 2.4 μm horizontally and 3.2 μm vertically, and all pixels that emit light from the red, green, and blue (R, G, and B) of the display prototype are configured to have the same pixel pitch.

The limit of human vision is reported to be 60 cycles per degree. Thus, if more than 60 light–dark cycles occur at a viewing angle of 1°, humans would not be able to distinguish light and dark and would perceive an intermediate color instead.

For best quality, smartphones should be viewed from a distance of approximately 30 cm. The estimated distinguishable resolution is then approximately equal to 500 ppi and the visual acuity is 60 cycles per degree.

A person would not be able to distinguish between a zigzag arrangement and a stripe arrangement in such a display since it is not possible for the human eye to distinguish each pixel at a pixel density surpassing 5000 ppi.

Moreover, a zigzag arrangement allows for the pixels to form a square at 2 x 2 pixels (approximately 2500 ppi). Thus, the zigzag arrangement will have virtually no effect on visibility.

3.3 Panel Structure

Figure 5 shows the configuration of our display prototype, which has a resolution of 1280 x 720 pixels. The scan drivers surrounding the pixels consist of n-type OS-FETs, formed in the same layer and same process as the pixels' selection and driving FETs. Thus, the formation of all these components does not result in an increased number of process steps.

3.4 Specifications and Display Image

Table 1 reveals the specifications of the display prototype, which achieved a pixel density of 5291 ppi by using CAAC-OS FETs that are between 60 nm and 200 nm in size and by scaling down the sub-pixel pitch to 2.4 μm x 3.2 μm. The display prototype is designed with a frame frequency of 120 Hz for VR use.

Figure 6 shows an image being displayed on the display prototype.

4 CONCLUSION

We fabricated a high-resolution OLED display prototype with 5291 ppi by using CAAC-OS FETs as the backplane. CAAC-OS FETs can be scaled down and have exhibited their capability to control the electric current necessary for the small pixels in a display with a pixel density of more than 5000 ppi. There is a demand for 3-inch displays in VR applications, and the next challenge in our work would be to enlarge the screen size.

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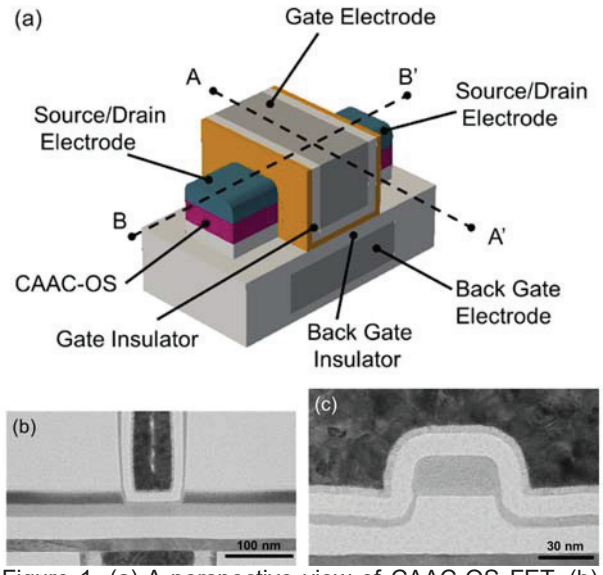
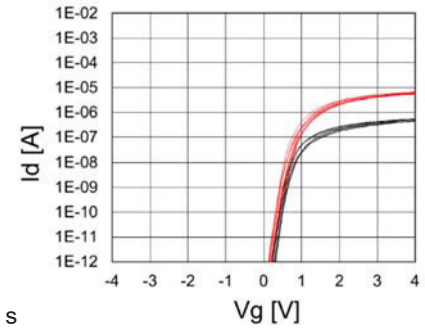
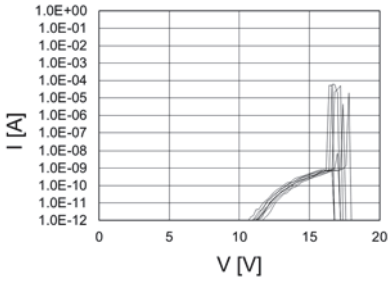


Figure 1. (a) A perspective view of CAAC-OS FET, (b) cross-sectional view of CAAC-OS FET in the A-A’ direction (channel length direction), and (c) cross-sectional view of CAAC-OS FET in the B-B’ direction (channel width direction)

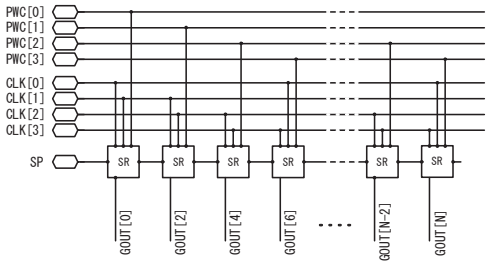


(a)

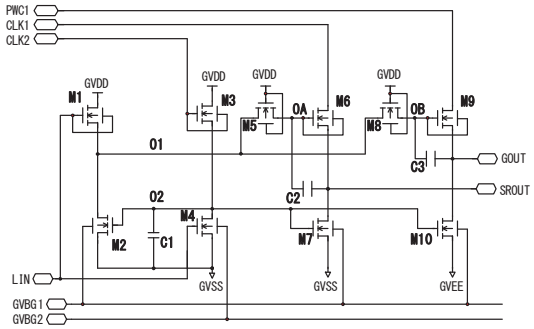


(b)

Figure 2. (a) Characteristics of a CAAC-OS FET with width and length equal to 60 nm. The sample size is 6 and Vds is set to 0.1 V (black line) or 1.2 V (red line). (b) Gate breakdown voltage.



(a)



(b)

Figure 3. (a) Block diagram of scan driver, and (b) shift register circuit.

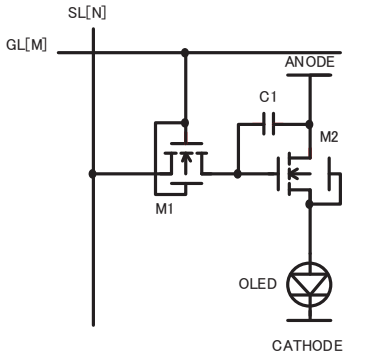


Figure 4. Sub-pixel circuit diagram.

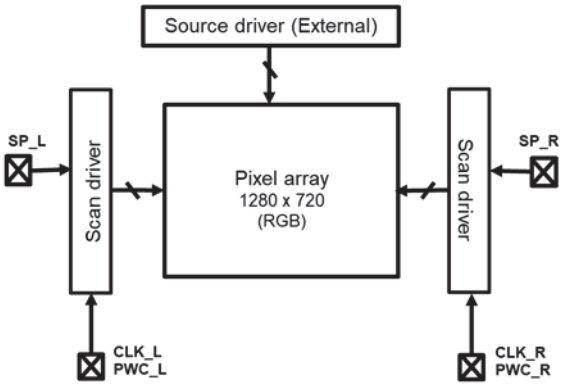


Figure 5. Display prototype configuration.

Figure 6. Image displayed on the display prototype.

Table 1. Display specifications

	Specifications
Screen diagonal	0.28 inches
Resolution	1280 x 720 (RGB)
Sub-pixel pitch	2.4 μm x 3.2 μm
Pixel density	5291 ppi
Emission type	Top emission
Frame frequency	120 Hz
Source driver	External
Scan driver	Integrated