Printing of 3D Electronic Circuits and Organic Thin-Film Transistors

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Keywords: Printed Electronics, Organic thin-film transistors, Metal nanoparticles

ABSTRACT

We propose a large-scale fabrication method of electronic devices based on solution-processed coating and printing. This method relies on bottom-up printing processes using soluble metal nanoparticles and organic semiconductors, resulting in thin-film electronic devices to be printed at room temperature without application of heat. We successfully fabricated high-performance organic thin-film transistors on plastic and paper substrates. In addition, the printing technique with 1-micron line width and space was also achieved. Our fabrication method is very promising for low-cost fabrication of high-resolution flexible electronics.

1 INTRODUCTION

Internet of things (IoT) is recently defined for the network to connect every single object, including displays, sensor devices and wearable devices. Basically, realization of these IoT devices requires the manufacture and integration techniques available in a large-area scale (2D extension) and in a multiple dimension (3D stacking) on a flexible substrate. In tradition, common electronic devices and circuits are fabricated using photo or electron-beam lithography, which despite being highly developed, still hardly satisfy the requirements in large-scale fabrication with certain resolution, use of flexible substrate, high-uniformity stacking for 3D configuration and environment-friendly production in a roll-to-roll process. Therefore, an alternative method instead of lithography has been highly concerned for developing high-performance flexible IoT devices.

In this sense, we propose the solution-based method for fabrication of electronic devices and circuits, which relies on bottom-up printing processes using soluble metal nanoparticles (NPs) and organic semiconductors as described in our previous publications [1-7]. We developed novel metal nanoparticle inks which can exhibit high conductivity without use of a sintering process [5]. We also developed the room-temperature (RT) printing technique which can assemble the nanoparticle inks into the desired configurations with high resolution [6]. In particular, our RT fabrication process allows use of flexible substrate without causing any thermal damages or deformation, resulting in highly-accurate layer-by-layer stacking for organic thin-film transistor (OTFT) fabrication. Thus, our fabrication method is very promising as a core technology for low-cost fabrication of flexible electronic devices. In this paper we report the materials and fundamental processes of our printing technique.

2 MATERIALS AND PROCESSES

We have developed the original metallic inks and high-resolution printing process for realizing room-temperature printing of electronics devices and circuits.

2.1 π-Junction Metal Nanoparticles

The critical difficulty in achieving a low-temperature fabrication process by printing is requirement of the high-temperature annealing process for sintering a common metal NP ink printed as electrodes. A conventional metal NP ink contains a non-conductive material as the ligand. High-temperature annealing is required to remove it and sinter the metal cores to obtain a conductive metal film. On the other hand, we developed π-junction NPs of gold and silver for the RT printing of the metal electrodes. The concept for this process and the principle behind the π-junction NP ink are shown in Fig. 1. The π-junction NPs possess a metal core surrounded by aromatic molecules as the conductive ligand as illustrated in Fig. 1a, which is the biggest difference between the new inks and conventional metal NP inks. The suspension of theπ-junction NPs in water can be used as the ink, and it can be deposited on a flexible substrate (Figures 1b and 1c). In the π-junction NPs, orbital hybridization between the π orbitals of the aromatic ligand and orbitals of the metal core improves charge transport among the NPs (Fig. 1d). Thus, conductive film can be obtained by RT deposition of the ink without removal of the ligand by annealing. The Au NPs clearly have a spherical shape that is maintained in the film (Fig. 1e). However, it exhibits low resistivity of ~9×10^{-6} Ω cm, which is of the same order of magnitude as that of pure Au of 2.2×10^{-6} Ω cm, without the sintering process because of the smooth charge transport among NPs through the conductive ligands. Thus, the metal NP film can be used as the electrodes for electronic circuits and devices. We can demonstrate the low- temperature coating of the Au NP ink on the plastic substrates, papers, and biomaterials substrates.

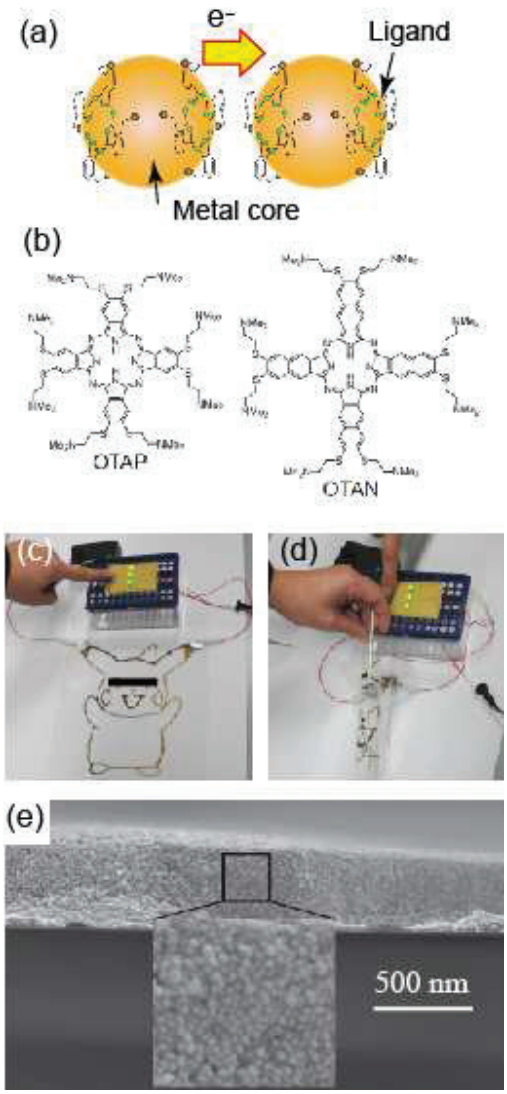

Fig. 1 π-Junction Metal Nanoparticles

(a) The schematic drawings of π-junction metal nanoparticles. (b) Typical molecular structure of π-conjugated ligands used for metal NPs. (c) Deposition of π-junction NP ink on a plastic sheet. (d) Flexing the π-junction metal NP ink printed on a flexible substrate. (e) Scanning electron microscope image of printed metal NP ink.

2.2 Selective Deposition of Metal NP Ink

In order to achieve high-resolution printing applicable for practical applications, we developed surface selective deposition technique. The high-resolution printing is performed on the hydrophilic/hydrophobic patterns induced by irradiation of vacuum ultraviolet (VUV, $\lambda < 200$ nm) light onto the hydrophobic polymer surface. The printing process is illustrated in Fig. 2a. First, the hydrophobic polymer surface was exposed to the VUV through a photomask to render the desired regions into hydrophilic. If we employ parallel VUV and irradiate it perpendicular to the substrate, we can obtain highly, homogeneously wetting domain arrays on the polymer surface with precisely defined boundaries between hydrophilic and hydrophobic regions. Deposition of NP ink can be performed on a coating stage, where ink droplets spread on the VUV-treated surface by a coating bar. The boundaries of wetting regions tightly pin droplet contact lines to retard film shrinkage, while the fluid films in dewetting regions spontaneously rupture to compensate the increased surface energy, consequently resulting in the precisely spontaneous patterning of high-resolution structures, like lines and gaps as illustrated in Fig. 2a.

As shown in Fig. 2b, fine patterns can be produced even in the case of complex circuits with a line width of 5 μm, which can be used for ultra-high-resolution sensors or detectors. Additionally, the prepared circuit lines ranging in width from 1 to 20 μm exhibit well-defined shapes, sharp edges, and a smooth surface (Fig. 2c). It is worth noting that such a high resolution of 1 μm exceeds the limitation (~2 μm) of conventional photolithography used in fabrication of liquid crystal displays.

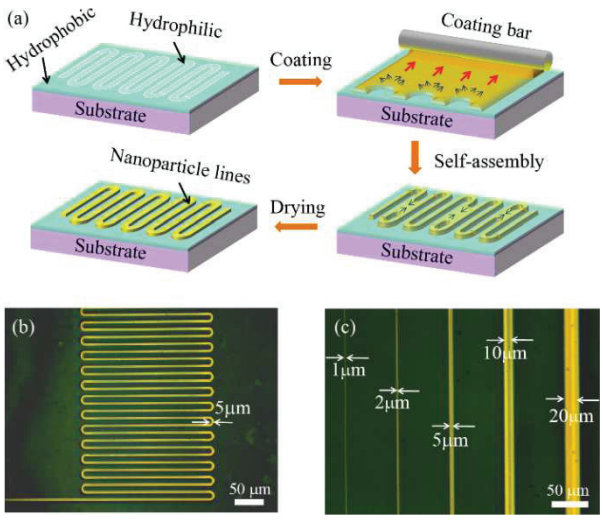

Fig. 2 Selective Deposition of Metallic Ink

(a) The schematic illustrations of surface selective deposition using π-junction NP ink. (b), (c) Optical microscope images of printed lines. Line width of 1 μm can be achieved.

3 ORGANIC THIN-FILM TRANSISTORS

Room-temperature printing process allows us to fabricate fully-printed organic thin-film transistors (OTFTs) with high-performance.

3.1 Fully-Printed OTFTs

For fabrication of the printed OTFTs using the Au NP ink, a stack of four layers, including source/drain, organic semiconductor, gate dielectric, and gate electrode layers,

was prepared to complete the devices, and the RT process was employed for all layers. The fabrication process of printed OTFTs is shown in Fig. 3a. We chose polyethylenenaphtalate (PEN) film with surface modification layer of Perylene-C as a flexible substrate. The hydrophobic substrate surface was then exposed to VUV through a photomask to form hydrophilic patterns. The Au NP ink was coated and selectively deposited onto the hydrophilic regions by bar coating to print out source and drain electrodes (Fig. 3a left). The printed Au bottom electrodes were directly used for further device application without any annealing or sintering process. Organic semiconductor layer of 2, 7-dioctyl[1]benzothieno[3, 2-b][1]benzothiophene (C_8-BTBT) was also patterned by selective solution casting onto the source/drain electrodes (Fig. 3a center). After formation of the gate dielectric layer by spin-coating, the VUV method was used again to form top gate electrodes (Fig. 3a right). The OTFT arrays printed on a flexible substrate is shown in Fig. 3b.

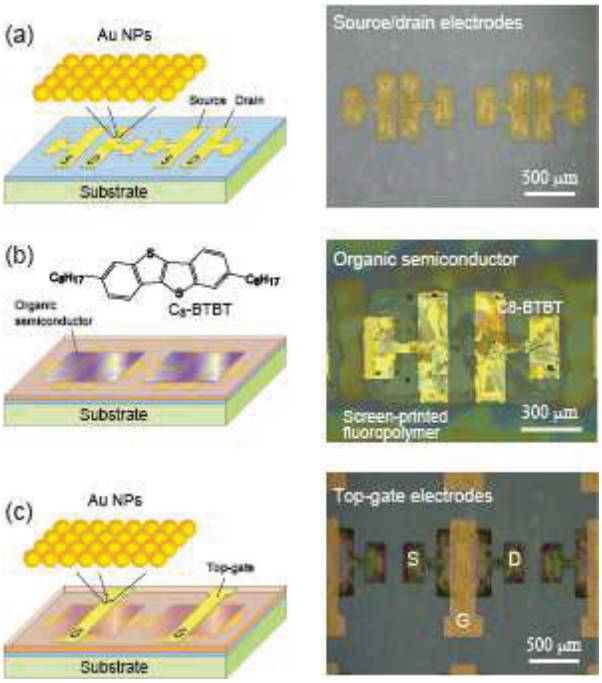

Fig. 3 Fully-Printed Organic Thin-Film Transistors
This figure represents the fabrication process of fully-printed OTFTs with metal nanoparticle ink. (a) Printing of source and drain electrodes by selective deposition of Au nanoparticle ink. (b) Deposition of organic semiconductor ink onto the channel regions. (c) Printing of top-gate electrodes with Au nanoparticle ink.

3.2 Device performance

The results of electrical characterization for the fully-printed OTFTs are shown in Fig. 4. The nonlinear increase in drain current in the low-drain-voltage region in the output characteristics (Fig. 4a) was attributed to the relatively high contact resistance at the metal/semiconductor interface. Since C_8-BTBT is wide bandgap material and the film has a deep valence band level (EV = 5.7 eV), a high charge injection barrier can exist at the metal/organic interface due to the energy mismatch between the Fermi level of the Au NP electrodes and the VB of the C_8-BTBT film. In contrast, the drain current in the high-drain-voltage regions shows saturation characteristics, which confirms an ideal MOSFET operation. Fig. 4b shows that hysteresis-free transfer characteristics were achieved with a steep increase in drain current in the sub-threshold region. Gate leak current was substantially reduced by complete patterning of the electrode and semiconductor layers, which allowed an on-off ratio of 106. The average field-effect mobility (μ_{FET}) and threshold voltage of the fully-printed OTFTs were 7.9 ± 1.1 $cm^2\ V^{-1}\ s^{-1}$ and 1.1 ± 0.4 V, respectively.

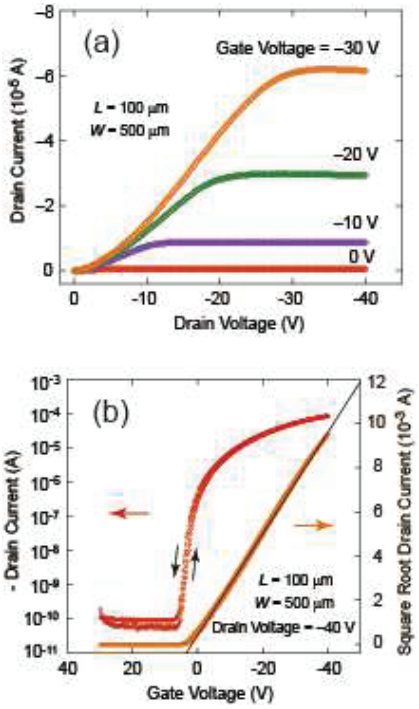

Fig. 4 Electrical Performance of Fully-Printed Organic Thin-Film Transistors
(a) Typical output characteristics of fully-printed OTFTs fabricated on a flexible substrate. (b) Typical transfer characteristics of fully-printed OTFTs.

4 CONCLUSIONS

We developed room-temperature fabrication process of electronic devices using high-resolution printing of metal nanoparticles and organic semiconductors. Using the surface wettability contrast defined by the VUV irradiation to the hydrophobic polymers, we achieved spontaneous patterning of narrow Au lines and gaps

down to the width of 1 micron, as well as discrete organic semiconducting thin films, which allowed the homogeneous integration of high-resolution electronic devices including short-channel OTFTs at a large scale. This spontaneous patterning strategy for scaling down the electronics, in combination with the homogeneous integration method, should be promising for fully solution-processed, lithography-free, large-area, high-resolution flexible devices.

5 ACKNOWLEDGEMENT

This work was financially supported by a Grant-In-Aid for Scientific Research (No. 26286040 and 15K21617) from the Ministry of Education, Culture, Sport, Science, and Technology of Japan, and a Grant for Advanced Industrial Technology Development (No. 11B11016d) from the New Energy and Industrial Technology Development Organization (NEDO), Japan, and also by Henan Province Nature Science Fund (No. 162300410261) and Distinguished Youth Developed Science Fund (No. F0001182). We extend our thanks to Nippon Kayaku Co. and Dr. Takimiya (RIKEN) for providing us with C_8-BTBT.

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