Integrated Polycrystalline Silicon Photomask Technology for Low-Temperature Polycrystalline Silicon (LTPS) TFTs

Jia-Hong Ye*, Ching-Liang Huang, Kuo-Yu Huang, Maw-Song Chen, Wen-Ching Tsai, Wei-Ming Huang, Yang-An Wu

AU Optronics Corporation, Hsinchu Science Park, Hsinchu 300, Taiwan, R.O.C.
***E-mail: JiaHong.Ye@auo.com**

Keywords: LTPS TFTs, hybrid backplane, LTPO

ABSTRACT

A novel Four-Photomask complementary metal oxide semiconductor (CMOS) technology for low temperature polycrystalline silicon (poly-Si) thin film transistors (LTPS TFTs) was proposed in the first time. The combination of poly-Si layer and P plus (P+) region definitions within one lithography process was realized by a half-tone photomask. In this paper, the characteristics of TFTs within a half-tone Poly-Si Photomask of lithography processes were reported and compared with electrical characteristics of typical Six-Photomask lithography processes. The Integrated Poly-Si Photomask Technology can be applied to reduce the numbers of photomask of making an IGZO and LTPS Hybrid TFTs Array.

1. INTRODUCTION

LTPS TFTs (Low temperature polycrystalline silicon thin film transistors) have been employed as pixel switches and peripheral circuits in active matrix liquid crystal display (AMLCD), and especially the shift register circuit using CMOS LTPS TFTs has lower power consumption than the circuit using single type of N type or P type LTPS TFTs. Moreover, the CMOS LTPS TFT has more functionality than single type of N or P type LTPS TFT. (e.g. Employing N and P type TFT are to form, static random access memory circuit (SRAM), memory in pixel (MIP) LCD, which has advantage in ultra-low power consumption.) However, the conventional CMOS array backplane of AFFS (Advanced Fringe Field Switching) LCD using LTPS TFT processes requires inherently ten photomasks in lithography processes as shown in Figure 1. The improvement of this technology is needed to reduce the numbers of photomask of lithography processes. Using P+ and N+ compensation (counter) doping and the half-tone Poly-Si Photomask integrated into one lithography process can reduce six photomasks to four in CMOS LTPS devices processes. In this study, we investigated the Half-Tone Poly-Si Photomask Integrated Method and lithography processes flow and analyzed results of transfer characteristics of four photomasks CMOS LTPS TFTs and compared with typical six photomasks one.

2. EXPERIMENT

2-1 Typical Flow for CMOS LTPS TFTs Fabrication

Buffer layer was first deposited by plasma-enhanced chemical vapor deposition (PECVD). N type channel (N type) and P type channel (P type) LTPS TFTs were then fabricated on buffer layer and an amorphous-Si layer of 43nm thick was deposited and crystallized into polycrystalline silicon film by excimer laser annealing. After defining the active region, the P plus (P+) region of P type TFT and N plus (N+) region of N type TFT were defined by ion doping with two lithography processes. Silicon oxide and silicon nitride thin films were deposited as the gate dielectric, and resulted in a dual layer insulator of equivalent oxide thickness (EOT)=62.4nm. Next, the metal gate electrode, Mo (200nm thickness), was deposited and patterned. After deposition process of the inter layer dielectric (ILD), Source/Drain (SD) metals were deposited and formed. Coating and photolithography process of the organic layer (or PL: planarization layer) for high aperture application was subsequently formed. Silicon nitride thin film was deposited as dielectric (or PV: Passivation layer) between pixel electrodes (ITO2) and common electrodes (ITO1). Finally, ITO2 was patterned as metal pads, which forms a typical flow LTPS TFTs array backplane of an AFFS LCD. [1][2][3][4][5][6]

2-2 Integrated Polycrystalline Silicon/P+ Doping Region within Half-Tone Photomask

In typical CMOS LTPS TFTs processes, the first lithography process is to definite the pattern of polycrystalline silicon and the channel types need two lithography processes to complete the definitions of N+ and P+ doping regions. In this study, the half-tone photomask can mainly make polycrystalline silicon patterned and P+ doping processes within one step photo exposure and photoresist stripping. And compensation N+ region definitions can be combined with the metal gate electrode photomask. Table 1 shows a comparison of CMOS LTPS TFT fabrication processes with the two process flows.

The integrated processes: After the crystallization of

amorphous silicon by the ELA (excimer laser annealing) process, a half-tone photomask was employed to form the different thicknesses of the photoresist. N+ region and pixel area are of the same photoresist thickness, and photoresist thickness of the capacitor region and P+ region are thinner than N+ region and pixel area. In these Four-Photomask lithography processes, the poly-Si etching process is critical. To avoid N type channel thin film transistors (N type TFTs) damaged by ion implantation of boron (P+ doping), the lateral etching process method was developed in this study. Figure 2 shows that half-tone photomask uses CrOx or MoSi films to make 3 to 30% transmittance and also has dark and clear area like normal photomasks. By conventional lithography process, we can obtain the targeted pattern, photoresist thickness and photoresist profile, but thickness of the photoresist in the selected areas will be thinned. Figure 3 shows optical microscope image of P type channel and N type channel TFTs after simultaneous patterning with a half-tone photomask. Channel length of P-type channel TFT is defined by dark area of half-tone photomask.

The depth of lateral etching is another important process parameter after defining the active region (poly-Si layer). Proper lateral etching depth can protect poly-Si layer in N type region of N type channel TFTs from being P plus (P+) doped after oxygen plasma treatment to reduce thickness of photoresist. The poly-Si under photoresist was over-etched by the two steps etching (pattern etching and lateral etching).

After poly-Si etching process including lateral etching , oxygen plasma treatment is used to reduce the thickness of photoresist to remove the thin photoresist areas, which are the capacitor area (storage capacitor) and the P+ region. Therefore, P+ region was naked by additional ashing process (or oxygen plasma treatment). Ashing time of oxygen plasma treatment cannot be increased without limitation because the channel length of P type TFTs becomes shorter with increasing time.

In next step, the P+ region was formed by ion implantation of boron into naked poly-Si layer. After oxygen plasma treatment, the photoresist above the N+ region becomes thinner, while the photoresist above the P+ region and capacitor is totally removed. However, the N+ region is still protected due to the overall coverage of photoresist on the N type channel TFT regions after lateral etching. After photoresist stripping, integrated Poly-Si and P+ Doping within half-tone photomask lithography processes were completed.

After the metal gate electrode, N+ region can be doping aligning the gate with the source and drain regions due to compensation (counter) doping to complete Four-Photomask lithography CMOS LTPS TFTs array backplane.

After finish S/D metals, the other consecutive process steps are the same as typical CMOS LTPS TFT processes of an AFFS LCD backplane.

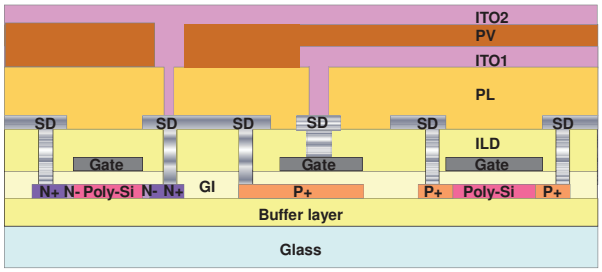


Fig. 1 Schematic cross-section of CMOS LTPS TFTs of an AFFS LCD backplane

Typical process flow		Integrated mask method	
PEP1	Poly	PEP1	Poly/P+
PEP2	P+		
PEP3	N+	PEP2	GE/N+
PEP4	GE	PEP3	VIA1
PEP5	VIA1	PEP4	SD
PEP6	SD	PEP5	VIA2
PEP7	VIA 2	PEP6	ITO1
PEP8	ITO1	PEP7	VIA 3
PEP9	VIA 3	PEP8	ITO2
PEP10	ITO2		

Table 1 Comparison of CMOS LTPS TFTs fabrication processes with typical processes and integrated photomask method flows in an AFFS LCD backplane

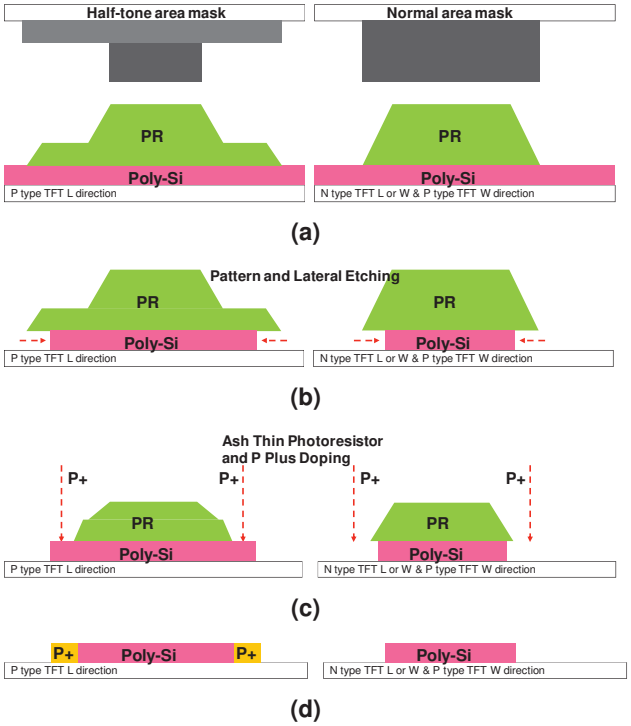
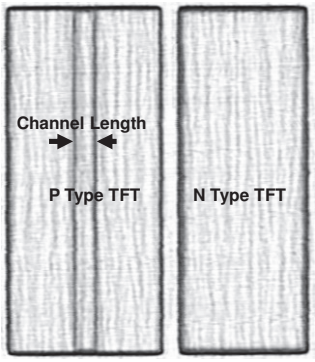
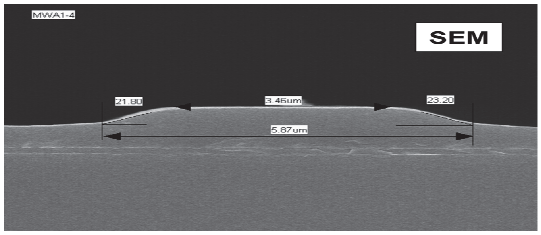


Fig. 2 Integrated Polycrystalline Silicon/P+ Doping within a half-Tone photomask (a) The different photoresist (PR) thicknesses with different regions after exposure with a half-tone photomask (b) Over etching to form lateral etching after poly-Si layer etching (c) Oxygen plasma treatment is used to remove the thin photoresist areas before P+ doping with ion implantation of boron (d) Poly-Si patterned and P+ doping regions after the Half-Tone Poly-Si Photomask Method.



(a)



(b)

Fig. 3(a) Optical microscope image of P type and N type channel TFTs after simultaneous patterning with the Half-Tone Poly-Si Photomask (b) Scanning electron microscope (SEM) image of P type TFT profile after one step photo exposure

2-3 Analysis Tools

Scanning electron microscope (SEM) and Optical Microscope (OM) were used for process analysis. The electrical characteristics of TFTs were measured by HP-4156C semiconductor parameter analyzer.

3. RESULTS AND DISCUSSION

3-1 Electrical Characteristics

Figure 4 shows the transfer characteristics of developed Four-Photomask CMOS LTPS TFTs with W/L=4.5μm/4.5μm. The electron mobility, subthreshold swing, and threshold voltage of an N type channel TFT were 48cm^2/Vsec, 0.2V/dec, and 0.6V. And the values of a P type channel TFT were 49cm^2/Vsec, 0.2V/dec, and -1.5V. However, the electron mobility with integrated method is lower than the typical one due to not proper for P+ doping of P type TFTs and N+ doping of N type TFTs corresponding to doping dosage optimization.

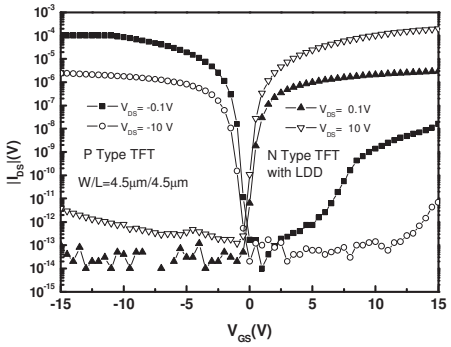
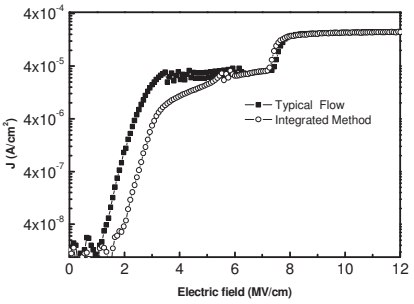


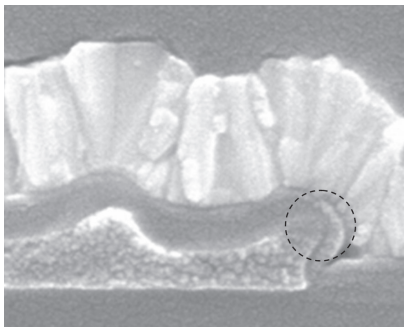
Fig. 4 Transfer characteristics of developed Four-Photomask CMOS LTPS TFTs with W/L=4.5 μ m/4.5 μ m

3-2 Comparison of Typical and Integrated Poly-Si/P+ Doping CMOS LTPS TFTs processes

Figure 5 shows Current Density-Electric Field (J-E) curves of gate insulator between P+ region of poly-Si layer and metal. The typical flow structure seems to have the lower leakage current and larger tunneling electric field. Leakage current result of the integrated method is larger than the typical flow structure about one order of magnitude in Table 2. These characteristics may be resulted from poor step coverage of gate insulator.



(a)



(b)

Fig. 5 (a) Current Density-Electric Field (J-E) curves of gate insulator between capacitor region (P+ region of poly-Si layer) and metal (b) Poor taper of poly-Si layer with over-etched process makes poor step coverage of gate insulator.

	Integrated Method	Typical Flow
$E_{breakdown}$	7.5 MV/cm	7.5 MV/cm
$E_{tunneling}$	1.75 MV/cm	2.00 MV/cm
$I_{leakage@2MV/cm}$	4E-7 J/cm^2	4E-8 J/cm^2

Table 2 Electric field and leakage of Current Density-Electric Field (J-E) curves

Figure 6 shows a comparison of transfer characteristic curves and gate metal leakages of Four-Photomask and Six-Photomask CMOS LTPS TFT devices. On current of four photomasks proces is lower than six photomasks process CMOS LTPS TFTs due to channel length variations and not appropriate doping dosage after Poly-Si/P+ Doping integrated method process. The larger leakage current is not contributed from gate current and this effect will be optimized further.

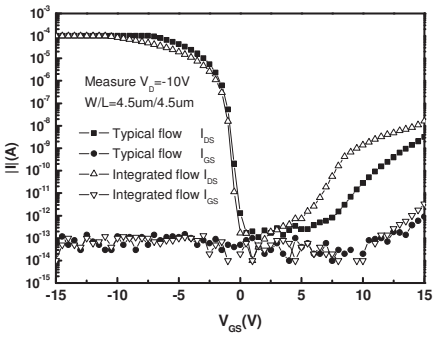


Fig. 6 Comparison of transfer characteristics curves and gate leakages between four photomasks and six photomasks CMOS LTPS TFT devices

Figure 7(a) shows schematic cross-section of P type LTPS and IGZO Hybrid TFTs array. IGZO TFTs as components of pixel switch can provide low leakage current and low power consumption with lower frame driving. [2][3][5][6] With IGZO and LTPS hybrid TFTs array technology in AMOLED pixel circuit, IGZO TFTs as components of switch TFTs can provide low leakage current power consumption and LTPS TFTs can provide high on current for OLED emitting period. However, this hybrid backplane needs ten-twelve photomasks to perform IGZO hybrid backplane array with LTPS TFTs. Applying the Half-Tone Poly-Si/P+ Photomask Integrated Method, P minus (P-) region can be doping aligning the gate with the source and drain regions to form the lightly doped drain (LDD) of P type TFTs with low leakage current and high reliability of hybrid TFTs array for reduced photomasks flexible OLED after the metal gate electrode.

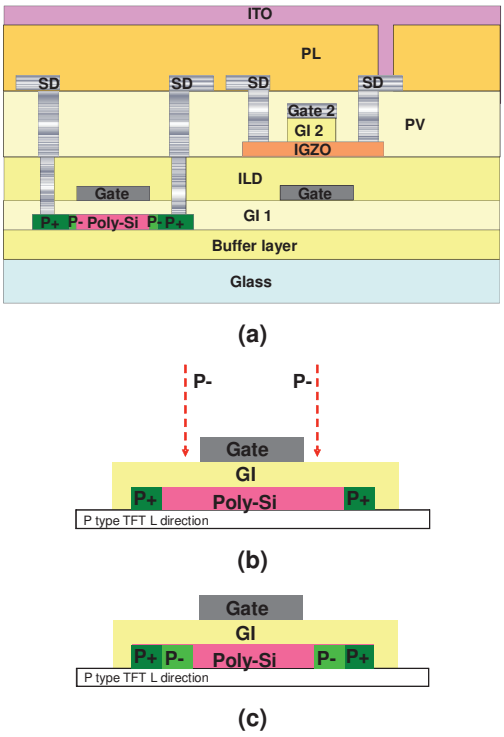


Fig. 7 (a) Schematic cross-section of top gate P type LTPS with top gate IGZO heterogeneous TFTs array (b) P- region can be doping aligning the gate to form the lightly doped drain (LDD) (c) Poly-Si patterned and P+ doping regions with the lightly doped drain.

4. SUMMARY

We have developed Four-Photomask CMOS LTPS TFT lithography processes with a half-tone photomask and three normal photomasks. The half-tone photomask combines the poly-Si layer and the P+ region definitions within one lithography process, which can reduce the production cost in mass production and this integrated technology is expected to apply in IGZO and LTPS Hybrid TFTs Array backplane technology.

5. REFERENCES

[1] J.-H. Ye et al., "Hot Carrier Stress for Low-Temperature Poly-Si TFTs with Various Widths" IDW of Technical Papers, AMDp - 14, 1753–1756 (2009)

[2] J.-H. Ye et al., "Reliability Improvement of IGZO and LTPS Hybrid TFTs Array Technology," SID Symposium Digest of Technical Papers, 12-4, 128–131 (2018).

[3] J.-H. Ye et al., "Development of Crystalline IGZO and LTPS Hybrid TFTs Array Technology" SID Symposium Digest of Technical Papers, 42-3L, 600-603 (2017)

[4] J.-H. Ye et al., "Development and Characteristic Analysis of Crystalline IGZO," SID Symposium Digest of Technical Papers, P-186L, 1213–1216 (2016).

[5] J.-H. Ye et al., "The Application of Crystalline IGZO TFTs for Utilizing a Hybrid Array Backplane LCD" IDMC of Technical Papers, S19-03 (2017)

[6] J.-H. Ye, "Heterogeneous TFTs Integration of IGZO and LTPS for A Display Backplane Technology" A Lecture in Short Course of SSDM 2018, Tokyo, Japan, Sep. 2018