Switching Characteristic Enhancement of p-type Cu_2O TFTs

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ABSTRACT

We propose three methods to enhance switching characteristics of p-type Cu_2O thin film transistors (TFTs) by passivating the copper oxide TFTs with silicon dioxide (SiO_2) using sputtering, oxidizing the back channel of copper oxide with hypochlorous acid (HClO), and doping gallium into the Cu_2O film.

1. INTRODUCTION

Amorphous oxide semiconductor (AOS)-based thin-film transistors (TFTs) have been a target of a considerable attention after the indium-gallium-zinc oxide-based TFTs were developed and announced worldwide by a research group led by Hosono et al [1]. According to that report, the AOS-based TFTs boast remarkable properties compared with widely used amorphous silicon (a-Si)-based TFTs including higher field-effect mobility (μ_{FE}), low off-current, and high transparency. As of today, the AOS-based TFTs are found in commercialized products such as organic light-emitting diode (OLED) displays. However, these extensive researches are limited only to n-type because most oxide semiconducting materials show intrinsically n-type characteristics. Furthermore, p-type oxide semiconductors have holes as carriers that move through the valence band maximum (VBM) which is formed by 2p orbitals of oxygen molecules. This forms many localized states that create heavy effective mass of holes, which cause low hole mobility in p-type oxide semiconductors. Also, oxygen vacancies that naturally form within oxide semiconductors generate electrons that work as trap sites for holes. Thus, only a few researchers have challenged to work on p-type oxide TFTs [2]. Nevertheless, these researchers are essential in developing high performing fully oxide-based complementary metal oxide semiconductor (CMOS) logic circuits to realize low power consuming and rapidly responding devices.

As one of the few representative p-type oxide semiconductors, copper oxides exist in two phases, cuprous oxide (Cu_2O) and cupric oxide (CuO), which have different electrical characteristics. Accordingly, there have been various researches to sought out appropriate copper oxide phase for p-type oxide TFTs. Yet, proper switching characteristics for p-type copper oxide TFTs have not been achieved compared with those of n-type AOS-based TFTs.

As following Fig. 1., in this study, we present three methods to enhance switching characteristics of p-type Cu_2O TFTs, which are passivating with silicon dioxide (SiO_2) to cause oxidation of CuO in back channel during annealing process, using hypochlorous acid (HClO) to oxidize the back channel [3], and doping gallium in channel to control oxygen vacancy. By adopting these techniques, we could successfully fabricate p-type oxide TFTs with improved electrical performances such as mobility and on/off ratio.

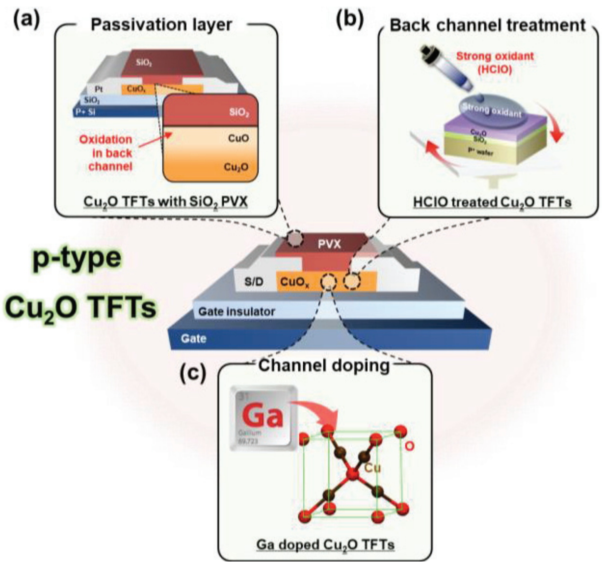

Fig. 1. Schematics of various techniques to enhance switching characteristics for p-type Cu_2O TFTs; (a) Cu_2O TFTs w/ silicon dioxide (SiO_2) passivation, (b) HClO treated Cu_2O TFTs, and (c) Ga doped Cu_2O TFTs.

2. EXPERIMENTAL

2.1 Fabrication method of SiO_2 passivated Cu_2O TFT

To fabricate Cu_2O TFTs, Cu_2O was deposited on a p^+-Si wafer with 120 nm thick SiO_2 using radiofrequency (RF) sputtering with 100 W RF power. After Cu_2O deposition, we annealed the device at 800˚C for 1 min in vacuum followed by Pt source and drain electrodes deposition by sputtering. Then, SiO_2 passivation layer was sputtered with 150 W RF power. Lastly, the device was annealed in air at 200°C for 30 min.

2.2 Fabrication method of HClO treated Cu_2O TFT

First, we prepared Cu_2O (0.2 M) solution by dissolving copper (II) nitrate hydrate $[Cu(NO_3)_2{\cdot}xH_2O]$ in 2-

methoxyethanol (2ME). Then, the Cu_2O thin films were spin-coated on a p^+-Si wafer with 120 nm thick SiO_2 followed by pre-annealing at 120˚C for 5 min. Then, the device was post-annealed at 500˚C for 1 h. Next, HClO solution was spin-coated onto the Cu_2O layer followed by annealing in air at 300˚C for 1 h. After repeating HClO coating/annealing 4 times, the films were rinsed with deionized water. Finally, Pt source and drain electrodes were deposited by sputtering.

2.3 Fabrication method of Ga doped Cu_2O TFT

For the fabrication of Ga-doped Cu_2O TFTs, we co-sputtered Cu_2O and Ga_2O_3 targets simultaneously on a p^+-Si wafer with 120 nm thick SiO_2 using RF sputtering. RF powers for Cu_2O and Ga_2O_3 targets were 100 W and 10 W, respectively. Then, post annealing at 800˚C for 1 min in vacuum was done to develop an active layer. Finally, Pt source and drain electrodes were deposited by sputtering.

3. RESULTS AND DISCUSSION

3.1 Results of SiO_2 passivated Cu_2O TFTs

First, the transfer characteristics of SiO_2 passivated Cu_2O TFTs are shown in Fig. 2 (a). It shows that the Cu_2O TFT without the passivation shows higher current values for both the on and off currents. However, when SiO_2 passivation was deposited by sputtering, the current level decreased significantly without any annealing. After the annealing at 200°C for 30 min, the switching property improved largely by decreasing the off current by the magnitude of 10^3 A. Therefore, the on-off current ratio improved from ~10^3 to ~10^8. As for Fig. 2 (b), it shows the output characteristics of SiO_2 passivated Cu_2O TFT that is annealed at 200°C for 30 min. As the data shows, the drain current is saturated for all applied gate voltages.

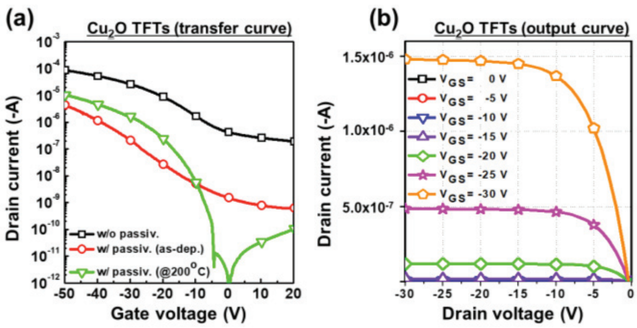

Fig. 2. (a) Transfer characteristics of SiO_2 passivated Cu_2O TFTs. (b) Output characteristics of SiO_2 passivated Cu_2O TFT annealed at 200°C for 30 min.

Fig. 3 shows the reason behind this switching property improvement. Firstly, when SiO_2 was deposited on top of the TFT, damage occurs due to sputtering. This damage breaks the bonds between Cu and O [4]. Thus, this induces formation of many defects such as weak Cu-O bonds, oxygen vacancies, etc. in the back channel, which is the top of the Cu_2O film. These defects act as hole traps that impede hole transport within the channel [5]. Thus, the overall current level is decreased.

Secondly, after the passivation, as the TFTs are annealed in the air at 200°C, CuO layer is formed at the back channel. This formation of CuO layer causes off current to drop significantly. Furthermore, as the damage is cured by the thermal annealing, the overall switching property is improved by also increasing the on current slightly.

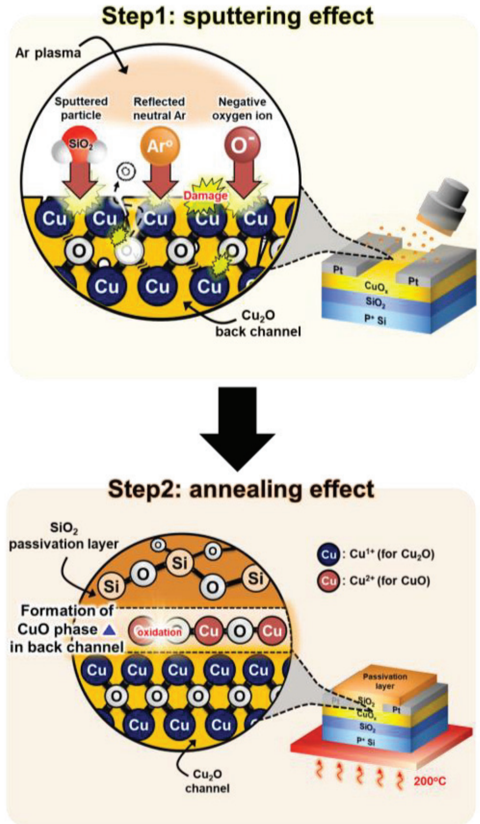

Fig. 3. The schematic illustration of the passivation effect on Cu_2O TFTs.

3.2 Results of HClO treated Cu_2O TFT

Next, we explore the effect of hypochlorous acid (HClO) oxidation on Cu_2O TFTs. Fig. 4 (a) shows the transfer characteristics of the HClO treated solution-processed Cu_2O TFTs. The Cu_2O TFT without HClO treatment that was annealed at 500°C showed poor switching property. However, for the HClO treated Cu_2O TFT, both the on and off currents decreased, where the off current dropped more significantly than the on current, thus improving the on-off current ratio from ~10^1 to ~10^4. As for the output characteristics of HClO treated Cu_2O TFTs that is shown in Fig. 4 (b), the drain current is shown to saturate at all applied gate voltages.

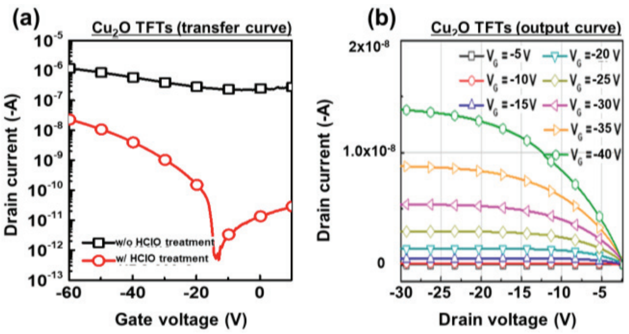

Fig. 4. (a) Transfer characteristics of HClO treated Cu_2O TFTs. (b) Output characteristics of HClO treated Cu_2O TFT [3].

Fig. 5 illustrates the reaction between HClO and Cu_2O film. Within the Cu_2O film, there are Cu vacancies that form when Cu enters the interstitial sites [6]. Therefore, when a strong oxidant such as HClO is applied on Cu_2O film, oxygen radicals that exist within HClO are highly likely to react with the Cu that exist at interstitial sites. This reaction between Cu and O form metal-oxygen bond that fill in the vacancies that are point defects of Cu_2O. Thus, both Cu vacancies and O vacancies decrease, and in turn, the switching property improves.

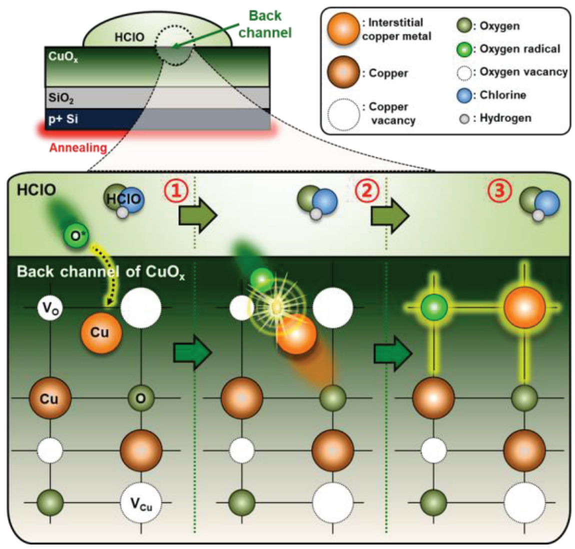

Fig. 5. Schematic for metal oxide formation and reduction of vacancies within Cu_2O film during HClO treatment [3].

3.3 Results of Ga doped Cu_2O TFTs

Finally, we engineered the channel layer by doping Ga inside Cu_2O TFTs. Fig. 6 (a) shows the transfer characteristics of Ga doped Cu_2O TFTs. As the graph shows, the non-doped Cu_2O TFT shows its on-off current ratio to be ~10^2. However, when Ga was doped, the on-off current ratio improved to ~10^4. For the output characteristics of Ga doped Cu_2O TFT shown in Fig. 6 (b), the drain current is saturated for all applied gate voltages.

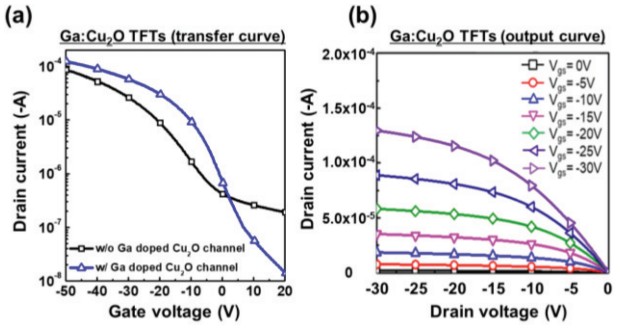

Fig. 6. (a) Transfer characteristics of Ga doped Cu_2O TFTs. (b) Output characteristics of Ga doped Cu_2O TFT.

Fig. 7 shows illustration of carrier conduction property before and after Ga is doped in Cu_2O film. Before Ga is doped, the existing oxygen vacancies impede the flow of holes as they act as hole traps. Therefore, the electrical performance is poor. However, when Ga is doped, oxygen vacancies are filled as Ga bonds well with oxygen. Thus, the holes flow smoothly within the film. Hence, this improves the switching property of the Cu_2O TFTs by increasing the on-current.

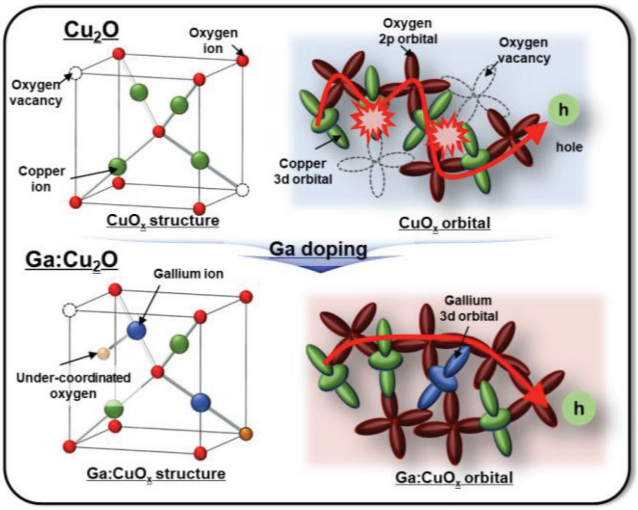

Fig. 7. Schematic illustration for conduction of Cu_2O before and after Ga doping.

4. CONCLUSION

In this paper, we investigated three method to improving switching characteristics of Cu_2O TFTs. From these researches, Cu_2O TFTs showed improved electrical characteristics compared with conventional Cu_2O TFTs. These approaches will allow p-type oxide TFTs to be adapted for CMOS application.

5. ACKNOWLEDGEMENTS

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