Simulation Study of Self-Heating and Edge Effects on Oxide-Semiconductor TFTs: Channel-Width Dependence

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ABSTRACT

We studied the channel-width dependence of oxide-semiconductor TFTs via a device simulator. The results show that the ON-current is affected by two factors: self-heating and edge effects. The former increases the current with a rise in temperature, while the latter produces the high edge current-density caused by its strong electric-field.

1 INTRODUCTION

Oxide-semiconductor thin-film transistors (OS TFTs) [1] are used for pixels, and horizontal- and vertical-driving circuits of flat-panel displays. The driving circuits use OS TFTs with large channel-width, *W*, at the output stage because the high current capability is required to drive heavy loads, such as gate-lines and data-lines.

When the large current flows in the OS TFT, its temperature increases self-heating based on Joule effects. The rise in temperature induces changes in electrical properties of the TFT [2, 3].

Most OSs are n-type semiconductors with carrier-electrons that show peculiar transport properties, such as the mobility increasing with an increase in the carrier density and temperature [4, 5]. Because of these transport properties, self-heating increases the current capability of OS TFTs. When the channel-length, *L*, of the OS TFT is shorter than 10 μm, the ON-current is higher than that derived from the simple size effect (*W*/*L*) and is described by the increase in the current capability via the self-heating [6, 7].

A goal of this study was to investigate the *W* dependence of OS TFTs using a three-dimensional (3-D) device simulator with the ability to incorporate the edge shape effect of potential and electric-field distributions near the edges along the *W* direction. As a result, we found that the device simulation considering the self-heating and edge effects reproduced the *W* dependence of the ON-current normalized by the TFT size, *W*/*L*. Thus, the dependence of the OS TFT size can basically be explained by the simple size, self-heating and edge effects.

2 SIMULATION MODEL

2.1 a-IGZO TFT

This study was based on the properties of OS TFTs with an amorphous In-Ga-Zn-O (a-IGZO) [1] channel layer. The a-IGZO TFTs had a bottom-gate and coplanar homo-junction source-drain (S-D) structure. The channel layer a-IGZO thickness was 40 nm and the gate-insulator SiO_2 thickness was 200 nm. The protection layer SiO_2 thickness was 200 nm, while the passivation layer SiN thickness was 200 nm. The TFT structure and basic properties were described in detail previously [8].

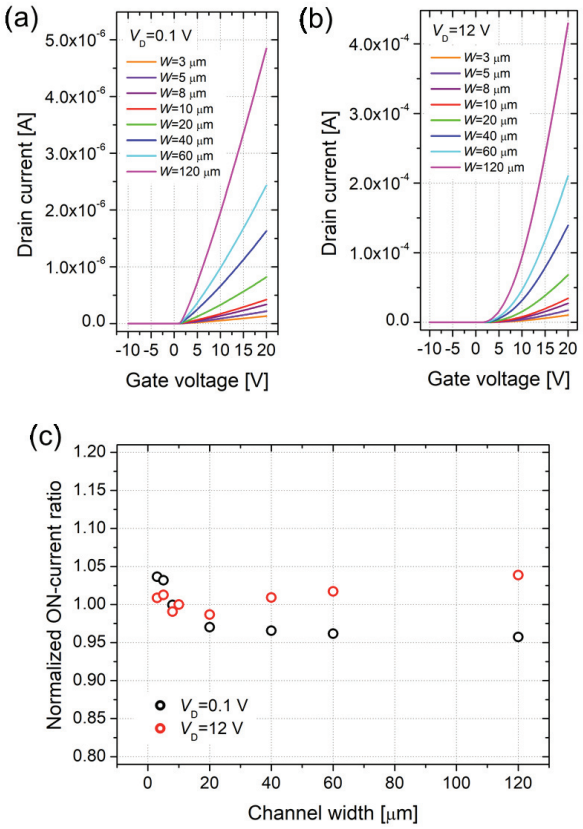

Fig. 1 Measured properties of a-IGZO TFTs

Measured transfer curves of a-IGZO TFTs with L=10 μm and various W (from 3 μm to 120 μm) at (a) V_D=0.1 V and (b) V_D=12 V, and (c) W dependence of normalized ON-current ratios (black open-circles: measured ratios at V_D=0.1 V, and red open-circles: measured ratios at V_D=12 V).

Figs. 1 (a) and (b) show the measured transfer curves of the a-IGZO TFTs with L=10 μm and various W (from 3 μm to 120 μm) at V_D=0.1 V and 12 V, respectively. The drain current, I_D, increased with increasing W.

A normalized ON-current ratio was the ratio of the normalized ON-current to that of the TFT with W=10 μm, where the normalized ON-current was defined as I_D normalized by W/L when the gate voltage, V_G, was 20 V. Fig. 1 (c) shows the W dependence of the normalized ON-current ratio. In the case of V_D=0.1 V, the ON-current ratio monotonically lowered with increasing W and was saturated around 0.95. In the case of V_D=12 V, the ON-current ratio lowered with increasing W in the range of W≤20 μm. In contrast, the ratio rose with increasing W in the range of W>20 μm and the maximum value was around 1.05.

2.2 Device model

Fig. 2 (a) shows a 3-D a-IGZO TFT structure diagram for this simulation study, while Figs. 2 (b) and (c) present the cross-section diagrams of the structure along the channel and the width direction, respectively. Two W edges appeared at both ends of the channel-width in Fig. 2 (c).

The 3-D simulator (VICTORY DEVICE, Silvaco Inc. [9]) employed a device model based on previous studies [6, 7]. The model included a-IGZO material parameters, density of sub-gap states, and a mobility model reflecting the carrier-electron transport characteristics of a-IGZO, such as increase of the mobility with the rise of temperature and carrier-electron density. The previous studies showed that 2-D simulation with the model can reproduce electrical properties of the long-channel a-IGZO TFT over a wide temperature range. Therefore, the 3-D simulation employing the device model was suitable for considering the self-heating and edge effects.

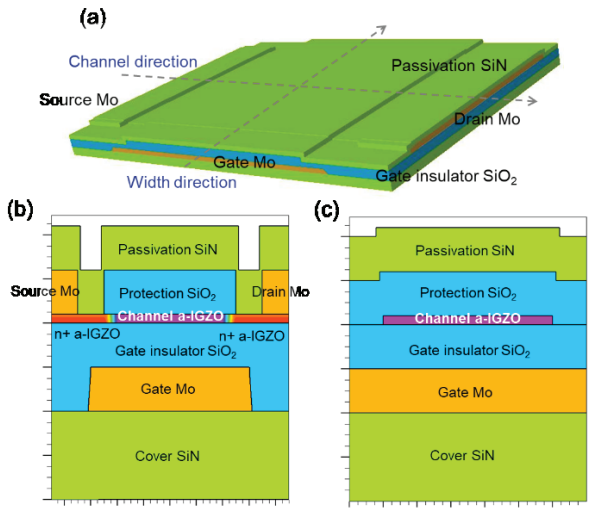

Fig. 2 Simulation structure diagrams of a-IGZO TFT
(a) 3-D structure diagram of a-IGZO TFT. (b) Cross-section diagram of the 3-D structure along the channel-length, and (c) cross-section diagram of the 3-D structure along the channel-width.

The thermal model is also required to estimate the self-heating effects. We used the general heat-flow equation with the heat generation and the thermal properties of a-IGZO reported by Yoshikawa et al. [10]. The heat generation was caused by the self-heating based on Joule heating. The thermal conductance and external temperature at the thermal boundary of the S-D electrodes were specified as 200 W/cm^2/K and 300 K, respectively.

3 RESULTS AND DISCUSSION

Fig. 3 (a) shows transfer curves at V_D=12 V calculated by the 3-D device simulator without the self-heating, while Fig. 3 (b) shows transfer curves at V_D=12 V calculated by the same 3-D device simulator with the self-heating. The difference between these transfer curves indicated that the self-heating clearly increased the ON-current.

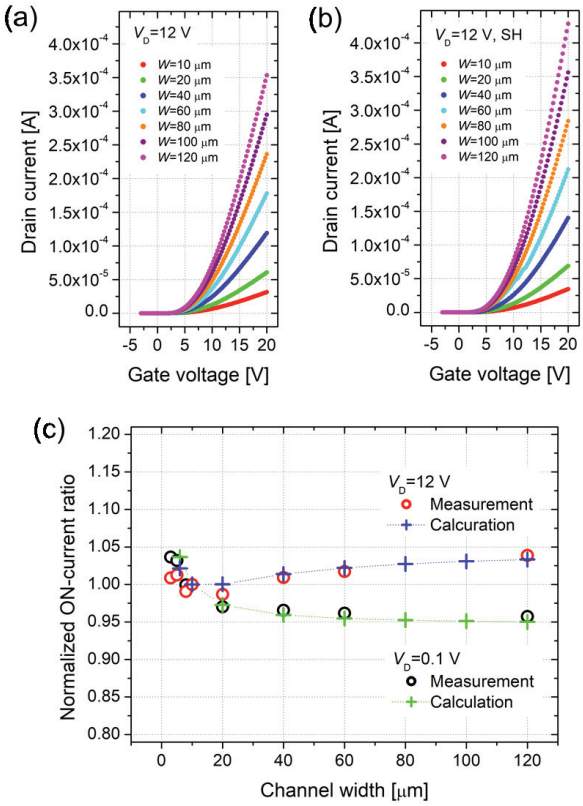

Fig. 3 Calculated properties of a-IGZO TFTs
Calculated transfer curves of a-IGZO TFTs with L=10 μm and various W (from 6 μm to 120 μm) at V_D=12 V (a) with self-heating and (b) without self-heating, and (c) W dependence of normalized ON-current ratios (black open-circles: measured ratios at V_D=0.1 V, red open-circles: measured ratios at V_D=12 V, green crosses with dotted-line: calculated ratios at V_D=0.1 V, and blue crosses with dotted-line: calculated ratios at V_D=12 V).

Fig. 3 (c) shows *W* dependence of the normalized ON-current ratios at V_D=0.1 V and 12 V (green and blue crosses) calculated with the self-heating, in addition to the measured ones (black and red open-circles) shown in Fig. 1 (c). The calculated ON-current ratio at V_D=0.1 V decreased with increasing *W* and the dependence was very close to the measured one. Similarly, the *W* dependence of the calculated ON-current ratio at V_D=12 V was very similar to the measured one which decreased with increasing *W* when *W*≤20 μm, and increased when *W*>20 μm.

In the case of V_D=0.1 V, the edge effect could be evaluated with no self-heating effects because of the low I_D. Figs. 4 (a) and (b) show the electric-field and the current-density distributions within the cross-section of the a-IGZO TFT along the *W* direction at V_G=20 V and V_D=0.1 V, where the TFT *W*/L was 10/10 μm and the position along the *L* direction was the *L* center. Because the areas near the both edges were affected by the gate outside of *W*, strong electric-fields appeared and led to the high current-density in the edge areas.

Assuming that I_D is composed of bulk current, I_{bulk}, and edge current, I_{edge}, where the former is the current proportion to the size (*W*/*L*) and the latter is the current flowing in the edge areas after the removal of I_{bulk} part, the ON-current, I_{ON}, is expressed by

$$I_{ON} = \left(\frac{W}{L}\right) I_{bulk} + I_{edge} \ .$$

In this case, the normalized ON-current ratio, R_{ON}, is described as

$$R_{ON} = \left(\frac{I_{bulk}}{I_{bulk} + I_{edge}}\right) + \left(\frac{L}{W}\right)\left(\frac{I_{edge}}{I_{bulk} + I_{edge}}\right) \ .$$

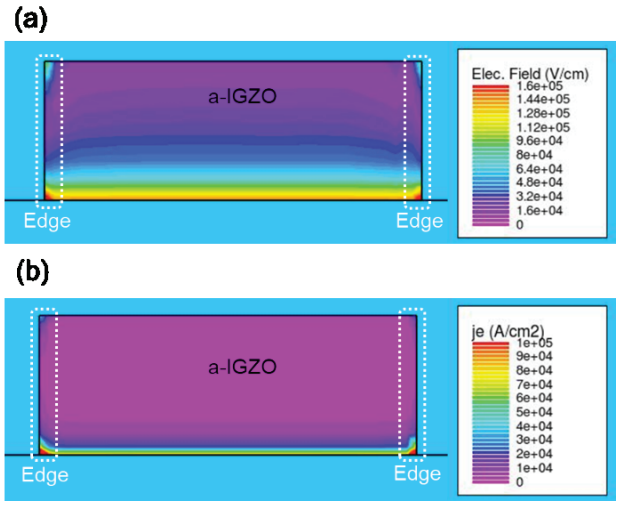

Fig. 4 Calculated electric-field and current-density distributions

Calculated (a) electric-field and (b) electron current-density distributions of a-IGZO TFT with *W*/*L*=10/10 μm at V_G=20 V and V_D=12 V.

Based on this assumption, I_{bulk}=3.66×10^{-7} A and I_{edge}=2.16×10^{-8} A were derived from the current-density distribution of the TFT with *W*/*L*=10/10 μm in Fig. 4 (b). Substitution of these values into the above equation showed that R_{ON} was around 0.95 when *W*/*L* is 120/10 μm. The value was almost the same as the measured one in Fig. 3 (c). The result indicates that the *W* dependence at V_D=0.1 V is explained by the edge effect.

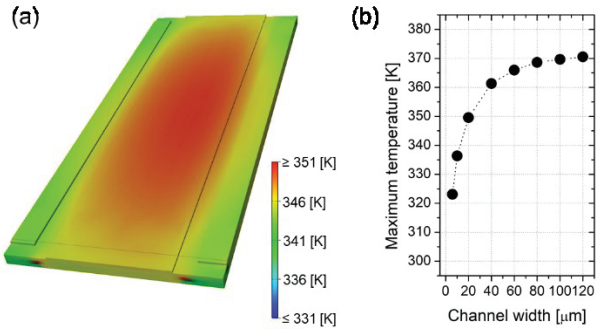

Fig. 5 Calculated temperature of a-IGZO TFTs

(a) Calculated temperature distribution of a-IGZO TFT with *W*/*L*=10/10 μm at V_G=20 V and V_D=12 V and (b) calculated maximum temperature of a-IGZO TFT with various *W* from 6 μm to 120 μm at V_G=20 V and V_D=12 V.

When V_D=12 V, the self-heating was active and the temperature distribution within the TFT appeared. Fig. 5 (a) shows the calculated temperature distribution of the a-IGZO TFT with *W*/*L*=40/10 μm at V_G=20 V and V_D=12 V. Because the highest electric-field along the *L* direction appeared near the TFT drain (not shown), the maximum temperature was observed near the drain. The temperature distribution is similar to the measured ones [2, 3], which supports the validity of the calculation.

Fig. 5 (b) shows the *W* dependence of the maximum temperature within the a-IGZO TFT with various *W* from 6 μm to 120 μm. The maximum temperature rose with increasing *W* and was saturated when *W*>80 μm. As described in the previous section, the increase in temperature also increases the current capability of the a-IGZO TFT because the mobility of the a-IGZO increases with the temperature. Consequently, when *W*>20 μm, the edge effect is small and the normalized ON-current ratio increases as *W* is wider. In contrast, when *W*≤20 μm, the ON-current ratio decreases with increasing *W* due to the low self-heating and large edge effects.

4 CONCLUSIONS

We studied the channel-width dependence of the OS TFTs via the 3-D device simulator employing the device model that can describe the peculiar carrier-electron transports. The 3-D simulation found that the edge effect caused the large current flowing near the channel-width

edges. Moreover, when the drain current is high, the self-heating increased the temperature of the device, which also increased the current capability of the TFTs according to the OSs' carrier-electron transport properties. Consequently, the ON-current calculated considering both the self-heating and edge effects reproduced the measured channel-width dependence.

This result indicates that the self-heating and edge effects can affect OS TFT operation. In addition, the degradation of the TFTs can be also impacted by these effects. Therefore, this simulation model would be useful to consider operation and degradation of OS TFTs.

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