

Nanostructured IGZO thin-film transistors with remarkably enhanced current density and on-off ratio

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ABSTRACT

We develop oxide TFTs with nanoscale and periodic degenerately doped heterostructures by using a strategy based on near-field nanolithography. These nanostructured TFTs remarkably enhanced in current density, compared with homogeneous IGZO TFTs. The on-off ratio was higher than 10^9 , with notably scaling effect with channel length.

1 INTRODUCTION

Thin-film transistors (TFTs) and field-effect transistors (FETs) are basic units to build functional electronic circuits and investigate transport physics. In conventional TFTs or FETs, performance in terms of current level, on-off ratio, and the sensitivity of detection is limited by homogeneous semiconducting layers. Recently, microstructures have been introduced to TFTs to offer better electrical properties and mechanical flexibility, such as wavy structures, nanogrooves, nanowires, and split structures.[1] Despite the advancements in TFTs with microscale microstructures, a general and versatile method to create sub-micron structures and interfaces to facilitate charge transport or induce interfacial effects is still lacking. For practical applications, TFTs yielding a large output current and high device mobility (e.g., over $50 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$) are desirable to drive high-resolution displays or Virtual Reality with organic light-emitting diodes (OLEDs) or micro-LEDs.

In this study, we successfully developed high-performance nanostructured transistors with degenerate/non-degenerate heterojunctions by a simple but effective near-field photolithographic strategy to produce nanostructures on surfaces covering several square centimeters. By using an array of pristine total-reflective poly-dimethylsiloxane (PDMS) pyramids or trenches, light beams are diffracted or reflected by slopes until they focus to expose the underlying photoresist, generating sub-wavelength geometries as small as below 100 nm in width. Based on an oxide semiconductor (InGaZnO), the nanostructured TFTs exhibited output current and transconductance nearly 20 times higher than conventional TFT and, thus, a high on-off ratio ($> 10^9$).

2 EXPERIMENT

For active layers of the heterojunction, a 50-nm ITO was first deposited by direct-current (DC) sputtering, and was then patterned with sub-micron gaps by photolithography using

total reflective PDMS trenches (Fig. 1a). In PDMS mask with a periodic array of micro-pyramids or trenches, the normal-incidence light transmitted onto an underlying photoresist surface can take one of three possible paths, as shown in Fig. 1b. Normal-incidence ultraviolet (UV) light through the sidewalls is first reflected and then refracted to another pyramid or trench. With multiple refractions and reflections, light is mostly trapped inside the PDMS mask and generates a high-intensity area near the tip. Simultaneously, light through the apexes directly penetrates the substrate and forms high-intensity areas as small as the sizes of the apexes. Consequently, only the photoresist below the apexes is completely exposed, thereby producing periodic sub-wavelength nanostructures. The nanopatterned samples were then deposited on a 70-nm IGZO film through RF sputtering followed by conventional photolithography to define the region of the active layer. After annealing at 350 °C for 1 h, the source and drain electrodes consisted of 100-nm-thick Al deposited by ac sputtering through shadow masks.

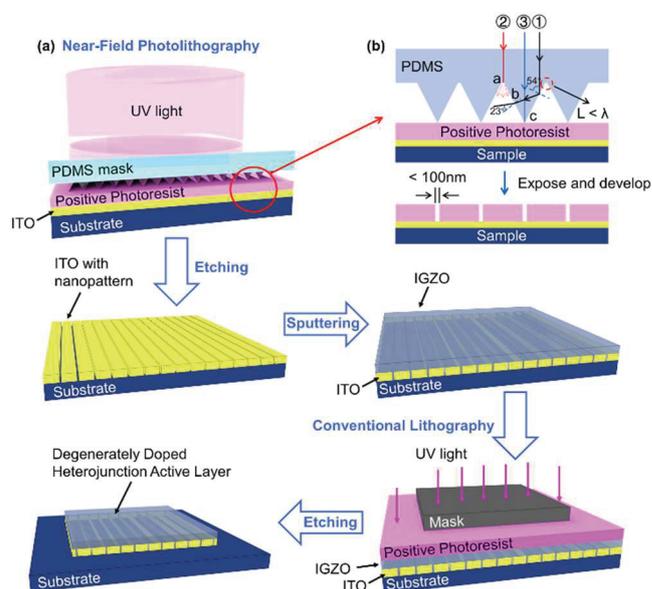


Fig. 1 The fabrication processes of periodic degenerately doped heterostructures active layer.[2]
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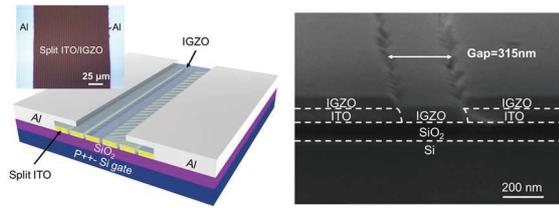


Fig 2. Schematic and SEM images of nanostructured heterojunction TFT.[2] Copyright 2019, ACS.

3 RESULTS AND DISCUSSIONS

3.1 Device structure

As shown in **Fig. 2**, these heterojunction TFTs are typical bottom-gate top-contact structure. The scanning electron microscopy (SEM) image shows that gaps between neighboring ITO strips were 315 nm wide. The subsequent IGZO film filled in the ITO nanogaps, which generated a vertical heterojunction through ITO to build the path of the current between the source and the drain electrodes.

3.2 Device performance

The electrical properties of the heterojunction TFTs are shown **Fig. 3a-c**. In both the linear and the saturated transfer scanning, the device exhibited strong gate tunability and high on-off ratio without observable hysteresis during forward and backward scanning. Devices with the proposed method using nanoscale and periodic heterojunctions achieved drain current I_D an order of magnitude higher than and off-current identical to the conventional TFTs with uniform IGZO channel layers, as shown in **Fig. 3a and 3b**. In the saturated regime (gate voltage $V_G = 40$ V and drain voltage $V_D = 40$ V), the drain current reached 17.5 mA, 17.5 times higher than that in the conventional IGZO TFT ($I_{Dmax} = 0.996$ mA). In the linear regime ($V_G = 40$ V and $V_D = 0.1$ V), a similarly large enhancement was obtained for I_D and transconductance $g_m = \frac{\partial I_D}{\partial V_G}$. The detailed relations between transconductance and differential apparent mobility with V_G are shown in **Fig. 3c**.

Note that these values are not the field-effect mobility of the active layer but the apparent mobility for the device, and can be regarded as the figure of merit for measuring the gate-tunability of conductance and the output current. When using the method of extraction of field-effect device mobility, the linear and saturated device mobilities were $165.8 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $144.2 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ (from fitting the slope of I_D and $\sqrt{I_D}$ against V_G , from $V_G = 25$ V to 40 V), respectively, both 17 times higher than those of conventional IGZO TFTs with $\mu_{lin} = 9.8 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ and $\mu_{sat} = 8.5 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$. If assuming ITO to be totally conductive, the *field-effect mobility* of the IGZO part was $16.6 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ (linear) and $14.4 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ (saturated).

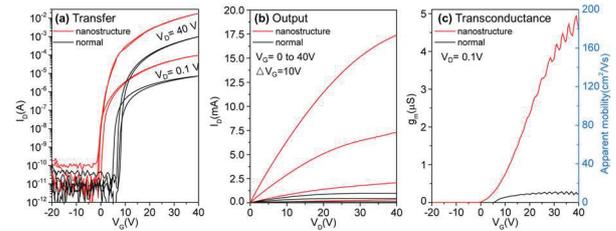


Fig 3. The electrical properties of devices with nanostructured heterojunctions channel or normal IGZO TFT. [2] Copyright 2019, ACS.

3.3 TLM result and scaling effect

We then investigated the scaling effect of channel length L for two reasons. First, the above interfaces between IGZO and ITO might have caused contact resistance to hinder transport as well as artifacts in gate-dependent conductivity. Second, although previous studies have used high-current oxide transistors by employing nanowires or partial capping layers, the scaling effect has rarely been studied even though it is important for practical applications and fundamental research.

Statistical data concerning devices with varied channel lengths L are shown in **Fig. 4**. The on-off ratios of devices with different values of L were 10^8 to 10^9 , and followed the relationship $I_{ON}/I_{OFF} \propto 1/L$. As both I_{ON} and I_{OFF} should ideally increase with $1/L$, such results indicate that the off current could be even lower than the lower limit in our measurements.

By varying L , we clearly observed the scaling effect as I_D increased with shortening L , as shown in **Fig 4**. In particular, the total resistance $R_{tot} = V_D/I_D$ exhibited a good linear relation with L . We calculated the channel resistance (R_{CH}) dependent on L and contact resistance (R_C) independent of L using the transmission line method (TLM) in the linear regime according to [3]:

$$R_{tot}W = R_CW + \frac{L}{\mu C_i(V_G - V_{TH})} \quad (1)$$

Here, μ , V_{TH} , and C_i , are the apparent device mobility, threshold voltage, and the capacitance of the gate dielectric per unit area, respectively. The extracted values of apparent device mobility at $V_G=40$ V was $161.3 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$ for the SiO_2 device, close to the values extracted from the transfer curves as shown above.

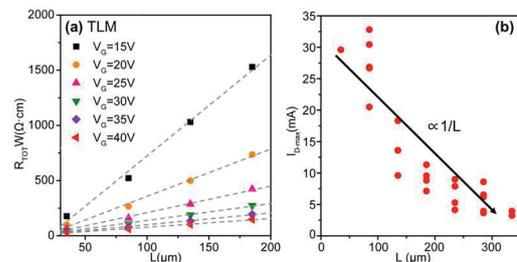


Fig 4. Results of TLM and the relation between maximum drain current and channel length.[2] Copyright 2019, ACS.

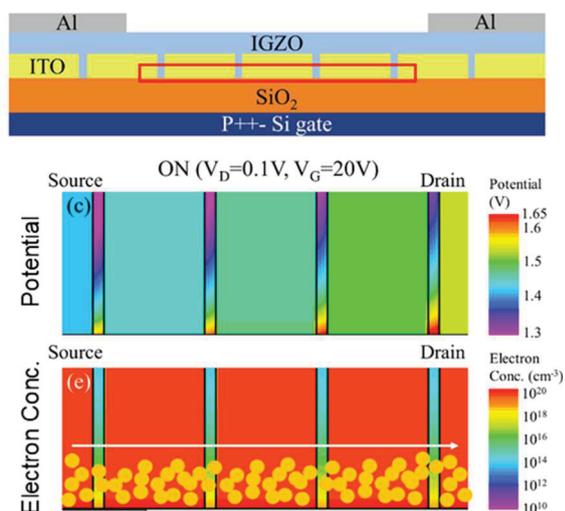


Fig 5. 2D device simulations of nanostructured degenerately doped heterojunctions of TFT.[2] Copyright 2019, ACS.

3.4 Device simulation

The operational mechanisms in the off or on states were quantified by 2D device simulations with computer-aided design (TCAD). The calculated potentials, carrier concentrations, and electric field are shown in **Fig. 5**. In the off state, the non-degenerate IGZO with low electron concentrations formed regions of space charge and induced built-in electric fields near the IGZO/ITO interfaces, which impeded electron transport and comprised the source–drain field. In the on state, the electron concentration in IGZO increased to form transport paths between the degenerate parts. Consequently, the drop in potential between source and drain mainly occurred in the IGZO parts, building up the periodic, large electric fields. The periodic heterojunctions confined a low off current at low gate fields and afforded a highly gate-tunable conductivity. In a control experiment, we exhibited changing gate-tunable conductivity by varying the length of the non-degenerate IGZO.

3.5 Compared with reported devices

We compared the proposed nanostructured TFTs with other reported oxide TFTs in terms of enhanced current and apparent device mobility. Dual active-layer TFTs have been proposed. They use a high-mobility semiconductor as underlying layer for transport and a low-carrier-concentration semiconductor material as top layer to guarantee a reasonable threshold voltage. A thicker underneath layer can induce high mobility and output current but sometimes may cause a negative shift in the threshold voltage and a low on/off ratio. A corrugated structure between InSnZnO (IZTO) and IGZO has been recently proposed to control the 2DEG with a dual active layer, and has yielded an apparent device mobility of 38 cm^2/Vs ($L = 50 \mu\text{m}$). The devices show a high on–off ratio, apparent device mobility, and obvious scaling effect.

Moreover, we compare the output current of these devices with the ideal TFT, *i.e.*, with constant mobility and zero V_{TH} , in **Fig. 6**. The normalized values of I_D for each reported device were obtained by dividing I_D with the corresponding C_i and $V_G V_D$ (for the linear regime) or $\frac{1}{2} V_G^2$ (saturated), and were compared with those of the ideal TFT with a series of mobility values (dashed lines). The normalized output current levels of the devices using the proposed strategy were among the highest, and reached the level of an ideal TFT with a constant mobility of $100 \text{ cm}^2/\text{Vs}$ and zero V_{th} .

4 CONCLUSIONS

In this study, we proposed nanostructured TFTs fabricated by using a facile, cost-effective, and high-throughput near-field photolithography technology. With nanoscale and periodic degenerate/non-degenerate heterojunctions, nanostructured TFTs exhibited 17.5 times the output current and transconductance than conventional TFT and, thus, a high on–off ratio ($> 10^9$) with notably clear scaling effect with channel length. This work can provide a platform for the investigation of interfacial effects at the nanoscale and functions in TFTs.

REFERENCES

- [1] L. Suhui, S. Jiyeong and J. Jin, “Top interface engineering of flexible oxide thin - film transistors by splitting active layer,” *Adv. Funct. Mater.* Vol. 27, No. 11, 1604921 (2017).
- [2] K. Huang, J. Wu, Z. Chen, H. Xu, Z. Wu, K. Tao, T. Yang, Q. Wu, H. Zhou, B. Huang, H. Chen, J. Chen, C. Liu, “Nanostructured High-Performance Thin-Film Transistors and Phototransistors Fabricated by a High-Yield and Versatile Near-Field Nanolithography Strategy,” *ACS Nano*, Vol. 13, No. 6, 6618-6630 (2019).
- [3] G. Horowitz, P. Lang, M. Mottaghi and H. Aubin, “Extracting Parameters from the Current - Voltage Characteristics of Organic Field - Effect Transistors,” *Adv. Funct. Mater.* Vol.14, No.11, (2004) 1069-1074 (2004).

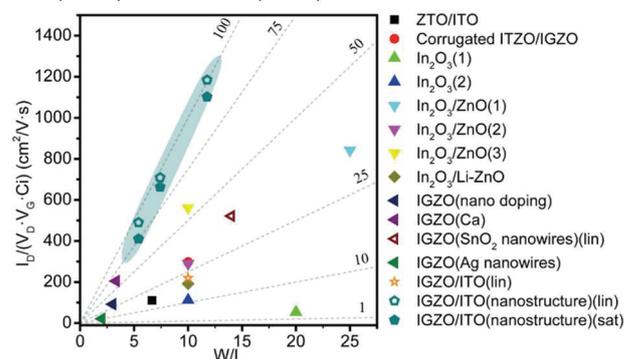


Fig 6. Comparisons in terms of output current between recently reported TFTs and the ideal TFT.[2] Copyright 2019, ACS.