

# Low-Temperature IGZO Technology on Transparent Plastic Foil by Atmospheric Spatial Atomic Layer Deposition

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## ABSTRACT

We use sALD to deposit IGZO and  $Al_2O_3$  layers in top-gated self-aligned TFTs, achieving a low-temperature process flow ( $\leq 200^\circ C$ ). We attain mobility of  $8\text{ cm}^2/Vs$  and switch-on voltage of  $-0.1\text{ V}$  for transistors with channel lengths down to  $1\text{ }\mu m$ , enabling a 200 ppi QVGA display on transparent PEN foil.

## 1 INTRODUCTION

The emergence of large-area electronics with novel form factors, such as rollable displays [1], transparent imagers [2] and skin-conformable health patches [3], requires processing of thin-film transistors (TFTs) on flexible substrates. Taking into account the demands in TFT performance, a widely explored combination is using metal-oxide semiconductors, such as sputtered Indium Gallium Zinc Oxide (IGZO), on plastic foils able to withstand high-temperatures, such as polyimide [4]. In order to enable applications where transparency of the substrate is key, as well as reduce manufacturing costs, it is desirable to process on transparent commodity foils such as polyethylene naphthalate (PEN), without compromising device performance.

Here we employ atmospheric plasma-enhanced spatial Atomic Layer Deposition (sALD), to deposit IGZO and aluminum oxide buffer layers, using a large-area sALD deposition process and prototype deposition tool

developed at Holst Centre [5]. The use of sALD allows processing the whole stack of co-planar top-gate self-aligned (SA) TFTs below  $200^\circ C$ , which in turn enables the use of PEN foil. The excellent uniformity and thickness control of sALD leads to high-performing TFTs, with an average field effect mobility of  $8\text{ cm}^2/Vs$  and a switch-on voltage of  $-0.1\text{ V}$ . Transistors with a channel length down to  $1\text{ }\mu m$  are achieved. We finally integrated the sALD IGZO-based SA TFT backplane with a top-emitting OLED and demonstrate a fully functional 200 ppi QVGA display.

## 2 BACKPLANE AND FRONTPLANE PROCESSING

The TFT processing in this work was based on the process flow employed before, using sputtered IGZO [6]. SA TFT backplanes with sALD were fabricated on 320 mm x 352 mm glass or PEN foil laminated directly on glass, on which a low-temperature ( $200^\circ C$ ) moisture barrier layer was deposited. The self-aligned TFT architecture [7] used is schematically presented in Fig. 1a. We used the pilot-scale sALD tool developed at Holst Centre (Fig. 1b), which features a fully automated sample transport system, a rapid thermal processing heating section and a sALD reaction chamber with a linear sALD injector head. This sALD tool design can achieve up to nm/s deposition rates for semiconductors and dielectrics.

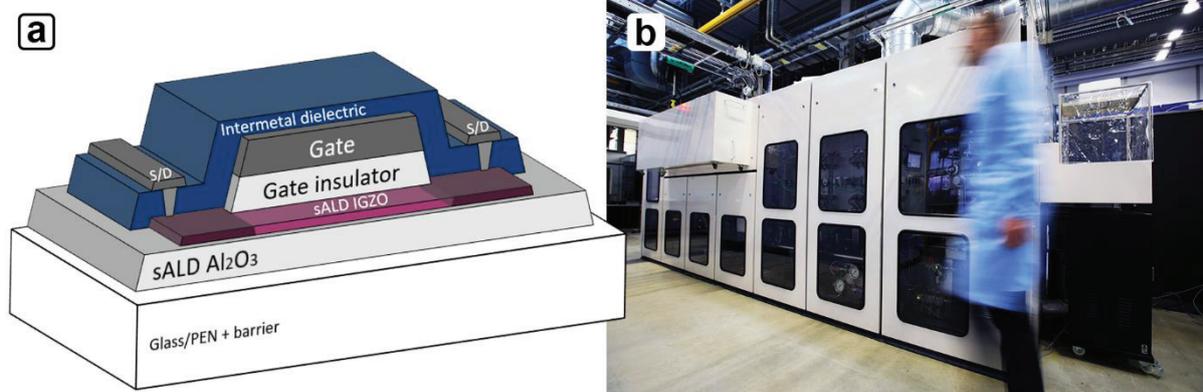
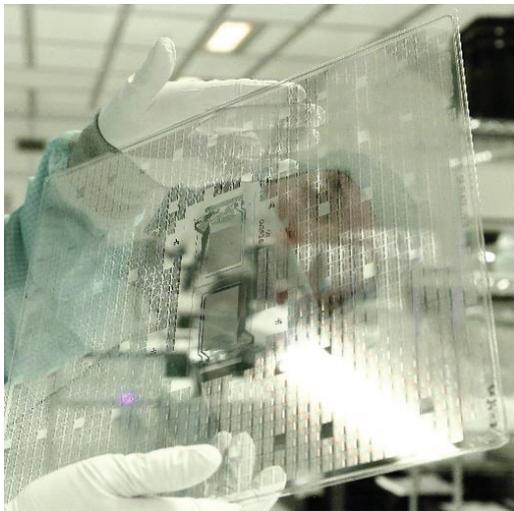


Fig. 1. a) Cross-section of a self-aligned TFT. b) Photograph of the pilot-scale sALD tool developed at Holst Centre.

The SA TFT fabrication starts with a full-area deposition of a sALD  $\text{Al}_2\text{O}_3$  buffer layer on top of the barrier on the PEN substrate. The 100nm aluminum oxide buffer layer was grown at a temperature of  $160^\circ\text{C}$ , using trimethylaluminum [ $\text{Al}_2(\text{CH}_3)_6$ , (TMA)] and an oxygen/nitrogen ( $\text{O}_2/\text{N}_2$ ) plasma as the aluminum and oxygen precursors, respectively. Immediately afterwards, the IGZO semiconductor layer is grown using sALD. Trimethylindium [ $\text{In}(\text{CH}_3)_3$ , (TMI)], triethylgallium [ $\text{Ga}(\text{C}_2\text{H}_5)_3$ , (TEG)], diethylzinc [ $\text{Zn}(\text{C}_2\text{H}_5)_2$ , (DEZ)], and an  $\text{O}_2/\text{N}_2$  plasma were used as the indium, gallium, zinc and oxygen precursors, respectively, at a temperature of  $160^\circ\text{C}$ . The final IGZO thickness employed in the TFT process was 15 nm. We have previously shown [5] that the thickness variation of the IGZO layer over the whole substrate area is less than 0.17 nm, demonstrating the unique uniformity capabilities of sALD over large(r) substrate sizes.

Following the deposition of IGZO, the layer was patterned using photolithography and no post-annealing treatment was applied. High-temperature annealing has been reported to increase performance in metal oxide semiconductors by removing anion-induced intrinsic defects, which can act as electron traps or shallow donor states [8]. We have observed that high performance is attained for sALD IGZO layers that have not been annealed at all, suggesting a low defectivity in the layer and highlighting the compositional control of the sALD technique.



**Fig. 2.** Photograph of the 320 mm x 352 mm substrate with laminated PEN foil. The 200 ppi QVGA IGZO TFT backplanes can be seen in the center.

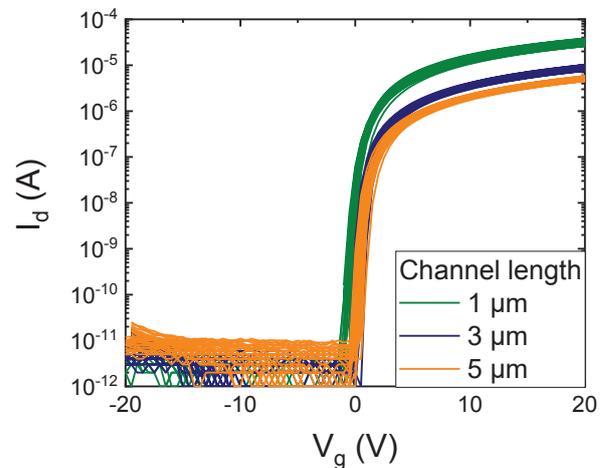
Afterward, a 200 nm  $\text{SiO}_2$  layer, deposited by PECVD at  $200^\circ\text{C}$ , and a sputtered molybdenum-chromium (MoCr) gate layer were deposited and patterned by photolithography. The patterned gate metal acts as the mask during the dry etching of the  $\text{SiO}_2$  gate insulator layer performed using Reactive Ion Etching (RIE). We

note that higher temperatures are typically employed for the deposition of good quality  $\text{SiO}_2$  with PECVD. Herein, we did not optimize the  $\text{SiO}_2$  recipe for the low-temperature deposition.

Subsequently, a 200 nm SiN inter-metal dielectric layer was deposited by PECVD at  $200^\circ\text{C}$ . This step also results in low-resistive IGZO contact regions that were exposed to the plasma during the PECVD process. Contact vias were photolithographically defined and dry etched in the SiN layer, after which MoCr source-drain electrodes were sputtered and photolithographically patterned. A photograph of the resulting TFT backplane is shown in Fig. 2. The plate contains 3.5 cm x 2.5 cm 200 ppi display backplanes (in the center) and process evaluation modules.

The SA TFT backplanes were further processed by depositing a hard baked interlayer, followed by a 100 nm MoCr OLED pixel anode layer. A second hard baked photoresist was used as pixel definition layer, preventing shorts between the anode and the transparent cathode. The (monochrome) OLED and transparent cathode were deposited through shadow masks and the display was completed by being encapsulated with a low-temperature thin-film barrier [9].

All process steps except sALD are industrial standards in FPD mass-production. All TFTs were measured in ambient using an Agilent 4155C semiconductor parameter analyzer connected to a semiautomatic prober.



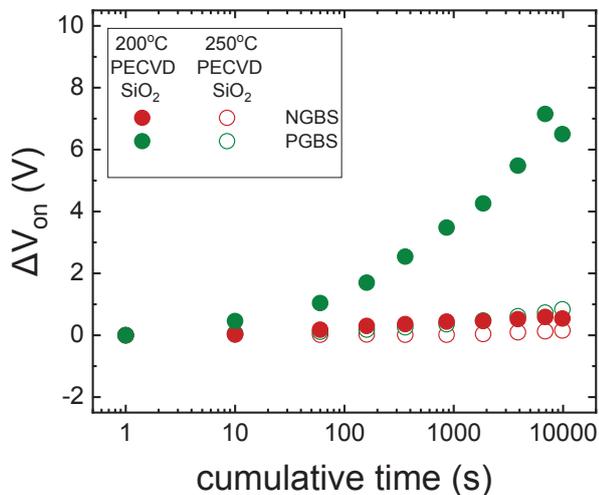
**Fig. 3.** Transfer characteristics,  $I_d$ - $V_g$ , of SA TFTs with 15 nm of sALD IGZO as the active channel material, deposited on a sALD  $\text{Al}_2\text{O}_3$  buffer layer. Forward and backward sweeps are shown but lie on top of each other. The channel width is  $10\ \mu\text{m}$ , while the channel length is  $5\ \mu\text{m}$ ,  $3\ \mu\text{m}$  and  $1\ \mu\text{m}$  for the orange, blue and green characteristics, respectively. The source-drain bias was 1 V.

### 3 RESULTS

#### 3.1 TFT PERFORMANCE

To evaluate the uniformity of the TFT electrical characteristics over the Gen1 plate, measurements were performed in a 4x5 matrix spanning the 320 mm x 350 mm substrate. The transfer characteristics of TFTs with a channel width,  $W$ , of 10  $\mu\text{m}$  and different channel lengths,  $L$ , are presented in Fig. 3. The TFTs exhibit good uniformity and hysteresis-free characteristics. The off-current is below 10 pA, while the on/off ratios exceed  $10^6$ . The average extracted linear mobility for the TFTs with a  $W$  of 10  $\mu\text{m}$  and an  $L$  of 3  $\mu\text{m}$  is 8  $\text{cm}^2/\text{Vs}$ , as extracted at  $V_g=20\text{ V}$ . This mobility value is on par with sputtered IGZO [5] and we have already demonstrated sALD-deposited semiconductors whose performance exceed that of sputtered IGZO, achieving a mobility of 30  $\text{cm}^2/\text{Vs}$  [10]. The turn-on voltage ( $V_{on}$ ), defined as the value of the gate bias for which the drain current is 100 pA, is -0.1 V. The subthreshold slope is ca. 315 mV per decade.

As it can be seen in Fig. 3, transistors with a channel length down to 1  $\mu\text{m}$ , the smallest allowed by the critical dimension (CD) of the photolithography employed, are operational. We have shown that the use of the  $\text{Al}_2\text{O}_3$  sALD buffer layer is important for achieving short channel length TFTs in our SA stack, as it can result in better control of the hydrogen content/diffusion in the TFT stack, alleviating the channel-shortening effect [5].



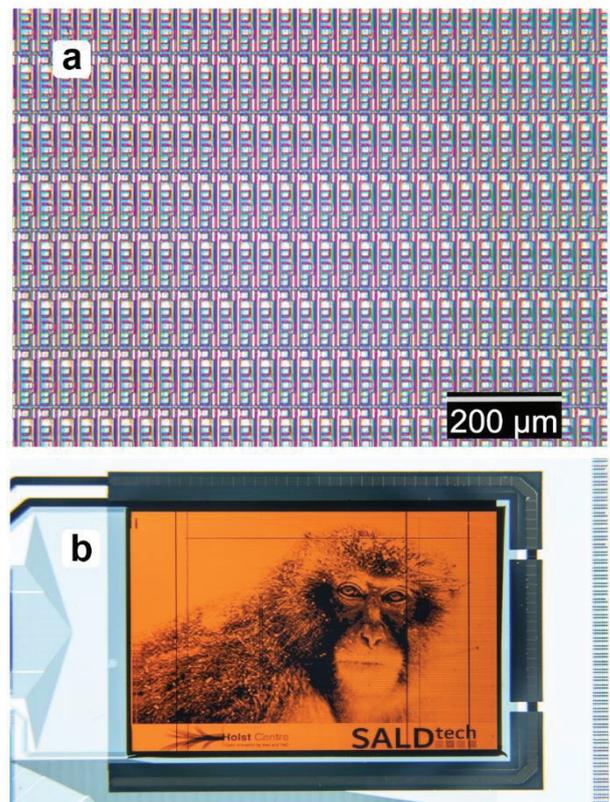
**Fig. 4.** Bias stress of sALD IGZO SA TFTs, represented by the change in switch-on voltage,  $\Delta V_{on}$ , for both positive and negative gate bias stress, as a function of the cumulative stress time. Pristine TFTs were stressed by applying a gate bias of  $\pm 20\text{ V}$ , corresponding to a field of  $\pm 1\text{ MV/cm}$  over the 200 nm  $\text{SiO}_2$  gate dielectric. Solid and open symbols are for a 200°C and 250°C PECVD  $\text{SiO}_2$  gate insulator layer, respectively.

#### 3.2 BIAS STRESS STABILITY

The bias stress stability is important for reliable operation of OLED displays. We therefore carried out

positive and negative gate bias stress (PGBS and NGBS, respectively) measurements on dedicated TFT test structures flanking the OLED display on glass. The measurements were performed at room temperature on transistors with a  $W/L$  of 15/5  $\mu\text{m}$  in air and under ambient light, after the source-drain metal deposition, prior to further passivation/encapsulation. An electrical gate field of 1  $\text{MV/cm}$  was applied for in total 10,000 seconds. Transfer characteristics were measured intermittently to determine the switch-on voltage.

The change in switch-on voltage,  $\Delta V_{on}$ , as a function of the cumulative stress time is presented in Fig. 4 for PGBS and NGBS, by the solid symbols. The positive gate bias stress after a cumulative stress time of 10,000 s is quite significant, reaching 6 V, while the negative gate bias stress is  $< 500\text{ mV}$ .



**Fig. 5.** a) Optical micrograph of the 200 ppi TFT backplane based on SA sALD IGZO transistors. The scale bar is indicated. b) The fully integrated QVGA AMOLED display, displaying a photo of a Japanese macaque (*macaca fuscata*) of Jigokudani, Yamanouchi, Nagano Prefecture (©2017 Ilias Katsouras).

We note that in this experiment an unoptimized, low-temperature PECVD  $\text{SiO}_2$  gate dielectric was deposited on top of the sALD semiconductor layer. We therefore expect that the observed bias stress behavior is not inherent to the sALD deposited material, but we ascribe it

to a poor interface between the semiconductor and the gate insulator. In support to this hypothesis, we include in Fig. 4 data of the same sALD  $\text{Al}_2\text{O}_3$  and sALD IGZO stack with our standard 250°C PECVD  $\text{SiO}_2$  gate insulator. As it can be seen, in this case the gate bias stress, both negative and positive, is much smaller, indicating that the observed bias stress in the low-temperature stack is related to the PECVD  $\text{SiO}_2$  and not the sALD layers. The bias stress can be improved upon optimization of the PECVD  $\text{SiO}_2$  deposition or, as envisioned by Holst Centre, by replacing this layer with a sALD-deposited gate insulator [11], reducing further the maximum process temperature for the whole TFT stack.

### 3.3 sALD IGZO-BASED DISPLAY

Fig. 5a shows an optical micrograph of the 200 ppi TFT backplane based on SA transistors with sALD IGZO as the active material. A photo of the final, fully integrated 200 ppi QVGA AMOLED display in operation is shown in Fig. 5b.

## 4 CONCLUSION

We have demonstrated the use of the pilot-scale atmospheric spatial Atomic Layer Deposition tool developed at Holst Centre to deposit IGZO semiconductor and  $\text{Al}_2\text{O}_3$  dielectric layers at low temperature, to fabricate high-performance, co-planar self-aligned TFT backplanes on commodity PEN foil. The sALD IGZO-based TFT backplane was integrated with a top-emitting OLED frontplane to fabricate a fully functional 200 ppi QVGA AMOLED display. The work highlights that atmospheric, low-temperature deposition as well as the reduction of the throughput time by sequential processing of sALD dielectric and semiconductor layers, make sALD a viable deposition technology for high-quality material layers for the FPD industry.

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