A Novel OLED Pixel Circuit with Controllable Threshold Voltage Compensation Time

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ABSTRACT

This paper proposes a novel pixel circuit that adopts low temperature polycrystalline silicon thin-film transistors (LTPS TFTs) to compensate deviation of threshold voltage (V_{TH}) of the driving TFTs (D-TFTs) and uses overlapping compensation times (T_{COM}) to extend the period of precise sensing V_{TH} variation of the D-TFTs in each pixel. Simulation and experimental results demonstrate the proposed pixel circuit under 120 Hz Ultra High Definition (UHD) driving condition has the same compensation performance as the 60 Hz Full HD (FHD) driving condition. Therefore, the proposed pixel circuit is suitable to be used in AMOLED display with high resolution and high-frame rate and can realize uniform OLED current (I_{OLED}) with high immunity to V_{TH} variation of the D-TFTs.

1 INTRODUCTION

Active matrix organic light-emitting diode (AMOLED) displays have been commercialized and rapidly developed by electronics industry in recent years. The backplane of mobile AMOLED displays adopts low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) based on the excimer laser annealing (ELA) owing to their high mobility, excellent reliability and small layout area. However, LTPS TFTs inevitably suffer from threshold voltage (V_{TH}) variations that are caused by fluctuation of laser beam in the ELA process. Thus, many compensation methods have been proposed to solve this problem of non-uniformity [1]-[4]. In most cases, the compensation operation senses to the real V_{TH} of D-TFT and stores the sensed voltage in a storage capacitor, If the stored voltage is identical to the real V_{TH} of the D-TFT, then pixel circuit can provide a precise driving current and produce uniform displayed image. In mobile applications such as smartphone, a resolution has been constantly increased and a higher frame-rate driving has been required to improve the moving picture response time (MPRT) [5]-[7]. Increase in the resolution and frame-rate affects the compensation time (T_{COM}) of AMOLED displays. That is, the higher resolution, the shorter compensation time. From figure 1, we can see that the image quality of AMOLED displays gets worse as the compensation time decreases [5]. Among various compensation methods, the voltage programming method is now widely used in AMOLED displays than the current programming method because of

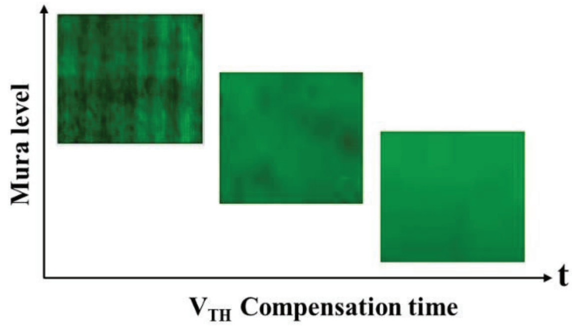

Figure 1. V_{TH} compensation time vs Mura level

a shorter compensation time, real-time compensation, and no need of additional external circuit [7]. In voltage programming method, most pixel circuit must use data line to provide reference or data voltage for pixels while they compensate for V_{TH} variations of D-TFTs. Since the data line in one row (1H) can only provide voltage within a scan time (T_{SCAN}), T_{COM} should be limited to T_{SCAN} or shorter than T_{SCAN}. However, as the required resolution and frame rate of displays increase, the T_{SCAN} of one row become shorter. That is, a short T_{SCAN} may cause the T_{COM} to be too short for the voltage programming method, resulting in the failure of compensation for non-uniformity brightness of a display image. To enhance the uniformity of a high resolution and high frame rate display, the T_{COM} should not be limited by T_{SCAN}. This paper proposes a new pixel circuit to compensate for V_{TH} variations of the D-TFT without using data lines, so T_{COM} can be extended which is longer than T_{SCAN}. This prolonging T_{COM} in each row guarantees an accurate detection of V_{TH} variations in the D-TFTs.

2 EXPERIMENT

Figure 2 shows schematic and timing diagram for proposed pixel circuit. This pixel circuit is composed of six p-channel TFTs and two storage capacitors. The operation of the proposed pixel circuit can be divided into a reset period, a compensation period, a data programming period (T_{PROG}), and an emission period. During a reset period, S2(n) goes low voltage, T2, T3, T4, and T5 are turned "ON". The voltage of node "A" is initialized to V_{DD} due to short current from

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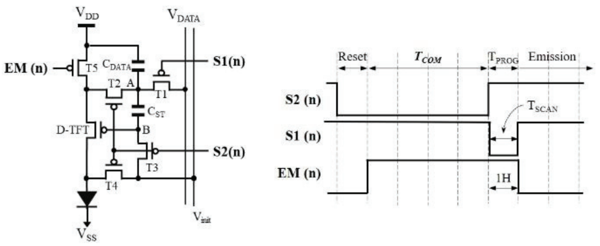


Figure 2. Schematic diagram (a) and timing diagram (b) of proposed pixel circuit

V_{DD} to the initial voltage (V_{init}). In addition, due to lower V_{init} than threshold voltage of OLED (V_{TH_OLED}), all currents that are generated by the D-TFT will flow into the V_{init} line rather than the OLED. Thus, the OLED remains in a completely dark state at this stage. During a compensation period, EM(n) goes high voltage, T5 is "OFF". At this time, the V_{TH} of D-TFT is stored at the storage capacitor (C_{ST}) by a diode connected D-TFT. Then, node "A" is discharging through T2 and T4 to yield a voltage written as,

$$V_A = V_{init} + |V_{TH}|, \quad V_B = V_{init} \tag{1}$$

During the data programming period, S2(n) goes high voltage and S1(n) goes low voltage, switch T1 is turned "ON" and switch T2, T3, T4, and T5 are turned "OFF". V_{DATA} is stored at the data storage capacitor (C_{DATA}) and gate voltage of D-TFT ($V_{G\_D\text{-}TFT}$) is boosted to V_{DATA} - $|V_{TH}|$ by C_{ST}. Therefore, $V_{G\_D\text{-}TFT}$ and V_{SG} of D-TFT ($V_{SG\_D\text{-}TFT}$) is written as

$$V_{G_D-TFT} = V_{DATA} - |V_{TH}|$$

$$V_{SG\_D-TFT} = V_{DD} - V_{DATA} + |V_{TH}| \tag{2}$$

Finally, during the emission period, S1(n) goes high voltage, EM(n) goes low voltage and T5 is turned "ON". During this period, D-TFT starts to saturate the output current by gate voltage of D-TFT stored in C_{ST} and C_{DATA} and the output current of D-TFT (I_{OLED}: OLED current) is given as

$$\begin{aligned} I_{OLED} &= \frac{1}{2}\frac{W}{L} C_{OX}\mu_P (V_{SG} - |V_{TH}|)^2 \\ &= \frac{1}{2}\frac{W}{L} C_{OX}\mu_P (V_{DD} - V_{DATA} + |V_{TH}| - |V_{TH}|)^2 \\ &= \frac{1}{2}\frac{W}{L} C_{OX}\mu_P (V_{DD} - V_{DATA})^2 \end{aligned} \tag{3}$$

According to Eq. (3), V_{TH} is eliminated, so the I_{OLED} is independent of V_{TH} of D-TFT. Therefore, the proposed pixel circuit can prevent I_{OLED} from influences of V_{TH} variations. From the timing diagram of figure 2, T_{COM} is not limited by T_{SCAN} where the voltage programming is implemented regardless of T_{SCAN}. Therefore, we can control the T_{COM} which is not limited by T_{SCAN} and compensation of multiple rows can be overlapped. Hence, pixel circuits generate uniform driving currents since there is enough time for compensating V_{TH} variation of the D-TFT. SmartSpice simulations are conducted and a test element group (TEG) of the proposed pixel circuit is fabricated to evaluate the performance of the proposed 6T2C pixel circuit. The aspect ratio of T1, T2, T3, T4, and T5 are 2.0 ㎛ / 3.0 ㎛ and D-TFT is 3.0 ㎛ / 12.0 ㎛ and capacitance of C_{ST} and C_{DATA} are 40 fF and 10 fF, respectively. The voltage of S1(n), S2(n) and EM(n) are from -7.0 V to 7.0 V. V_{DD}, V_{SS} and V_{init} are 4.0 V, -4.0 V and -5.0 V. The V_{DATA} range from 1.0 V to 5.0 V. Figure 3 plots I_{OLED} error rate versus V_{TH} variation of ±0.5 V corresponding with different T_{COM} and T_{SCAN}. In the conventional driving scheme, T_{SCAN} and T_{COM} are same time and the T_{SCAN} of FHD and UHD is 2.0 ㎲ and 8.0 ㎲, respectively. However, in the proposed pixel circuit, T_{SCAN} and T_{COM} are 2.0 ㎲ and 8.0 ㎲ when UHD driven. Details are given in figure 5 (a)-(c). From this simulation result, using the longer T_{COM} causes the proposed pixel circuit to sense variation of V_{TH} of the D-TFTs more precisely. As shown figure 3, the relative current error rates range from -28.6% to 26.4%, from -7.2% to 6.6%, and from -6.2% to 6.6% with different input timing conditions of the figure 5(a)-(c), respectively, conforming that the proposed 6T2C circuit with the longer T_{COM} of 8.0 ㎲ indeed compensates more effectively for TFT V_{TH} variations. T_{COM} of the proposed pixel circuit can be extended to above 20.0 ㎲ owing to its overlapping compensation.

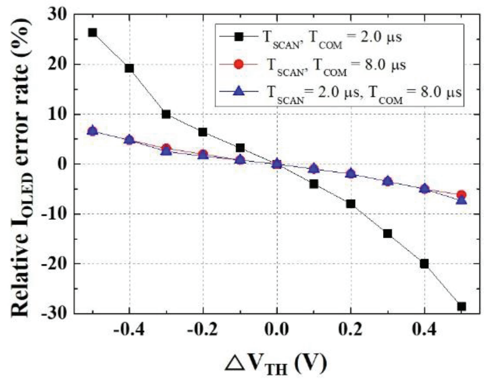
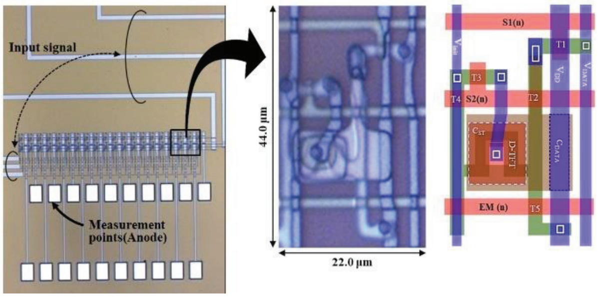


Figure 3. Simulation results of current error ratio with different T_{COM}.

3 RESULTS

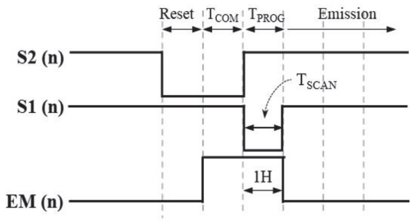
Figure 4 (a) and (b) show the layout and the photograph of the proposed pixel circuit TEG and unit pixel circuit with a pixel area of 22.0 ㎛ × 44.0 ㎛ in the fabricated panel, in which the positions of S1(n), S2(n), EM(n), V_{DD}, V_{init}, six TFTs and two capacitors are indicated. As shown figure 4 (b), the proposed pixel circuit presents effective compensation for 576 ppi high-resolution AMOLED displays. To evaluate the compensating performance of conventional driving and proposed pixel circuit, the anode voltage error rates with various T_{COM} are measured. We measured the anode voltage instead of OLED current due to the limit of a measurement equipment. Figure 5(a), (b) and (c) are input timing diagram with different T_{COM} and T_{SCAN}, respectively. Figure 6 shows anode voltage error rates and the standard deviations



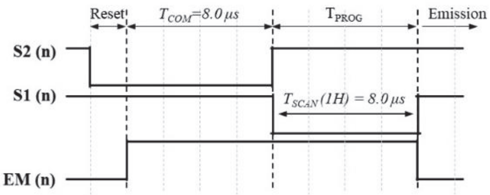
(a) (b)

Figure 4. Fabricated pixel array TEG (a) and unit pixel circuit with 576 ppi (b)

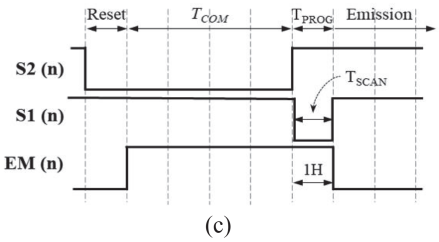
corresponding to figure 5(a), (b) and (c). The standard deviations of anode voltage for figure 5(a), (b) and (c) are 4.32, 0.87 and 1.03, respectively. Since the proposed pixel circuit can maintain or increase the T_{COM} even if T_{SCAN} is short, compensation performance equivalent to T_{SCAN} of 8.0 μs can be secured. Therefore, the above measurement results confirm compensation ability and high uniformity of D-TFT current of the proposed pixel circuit.



(a)



(b)



(c)

Figure 5. Input timing diagram, T_{SCAN} and T_{COM} = 2.0 μs (a), T_{SCAN} and T_{COM} = 8.0 μs (b), T_{SCAN} = 2.0 μs, T_{COM} = 8.0 μs (c)

So, the proposed pixel circuit has good image quality when used is the high- resolution display. Since the proposed pixel circuit cab be driven at high-frame rates, MPRT of the AMOLED display can be improved [7].

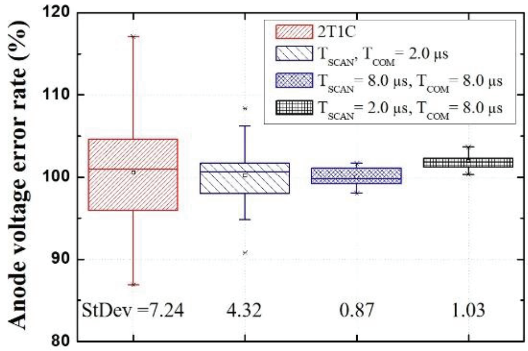


Figure 6. Measurement results with different compensation time with different T_{COM}

4 CONCLUSIONS

A novel 6T2C voltage-programmed AMOLED pixel circuit with controllable V_{TH} compensation time is proposed in this work. The proposed pixel circuit has excellent compensation ability on the V_{TH} variation of D-TFT though it is used in high resolution display which has a short scan time.

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