# a-IGZO TFT Gate Integrated Driver Circuit with AC-driven Pull-down TFTs for High Stability

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Keywords: Gate driver circuit, a-IGZO, Pull-down TFT, AC-driven, Duty ratio

**ABSTRACT**

*In the proposed gate driver circuit, pull-down TFTs are AC-driven with a duty ratio of 33.3% through CLK pulse instead of DC-driven through VDD power line. The simulation result exhibits output pulse of 1069th stage, 1071st stage, and 1073rd stage output pulse based on FHD, frame frequency of 120 Hz.*

## 1 INTRODUCTION

Amorphous-indium gallium zinc oxide (a-IGZO) thin-film transistors (TFTs) have attracted substantial attention for an active matrix organic light emitting diode (AMOLED) displays and active matrix liquid crystal display (AMLCD), such as a high-resolution, high frame rate display, and narrow bezels [1-4]. The a-IGZO TFTs have a low off-current, low temperature process, high on-off ratio, visible transparency and higher field effect mobility than amorphous silicon TFT [5]. For these reasons, gate driver circuit is mostly used based on a-IGZO TFT. The gate driver circuit generally applies a bootstrapping technique for the Q node to significantly increase the gate voltage of the pull up unit [6-7]. After this period, pull down unit is operated to discharge output node. However, the pull-down TFT is degraded due to the gate bias stress in the gate driver circuit [8]. The electrical characteristic degradation of the pull-down TFT may lead to the threshold voltage ($V_{th}$) shift and a decrease in the on-current. In the previous work, the method to drive pull-down TFT about output node through DC-driven (VDD) has been widely reported [9-12]. However, the DC-driven pull-down TFT is degraded due to continuous gate bias stress.

In this paper, we improve the overall reliability and stability of the circuit by designing new gate driver circuit based on oxide TFT for AMOLED and AMLCD. The proposed gate driver circuit is composed of three pull-down TFTs to sequentially discharge the output pulse using the CLK signals. Thus, it can prevent the $V_{th}$ shift due to degradation in the TFT. We used a method to drive pull-down TFT with duty ratio of 33.3% through AC-driven about output node. When the pull-down TFTs are sequentially operated, ripple voltage is almost not generated about output pulse in simulation. Circuit malfunctions caused by performance degradation of the pull-down TFTs can be improved through new gate driver circuit structure. We also simulated output pulse of 1069th, 1071st, and 1073rd gate line to verify the stability of the output voltage at FHD (1080 gate lines) in proposed gate driver circuit.

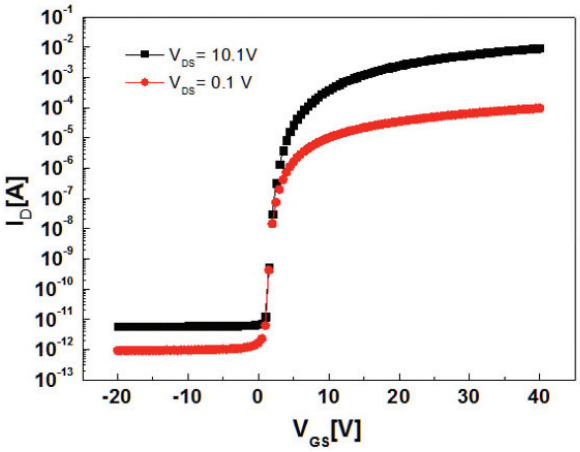
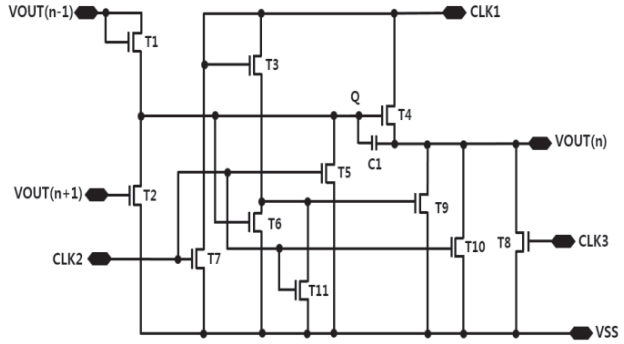



**Fig. 1 I-V characteristic of a-IGZO TFT (Pull-down TFT) in simulation**

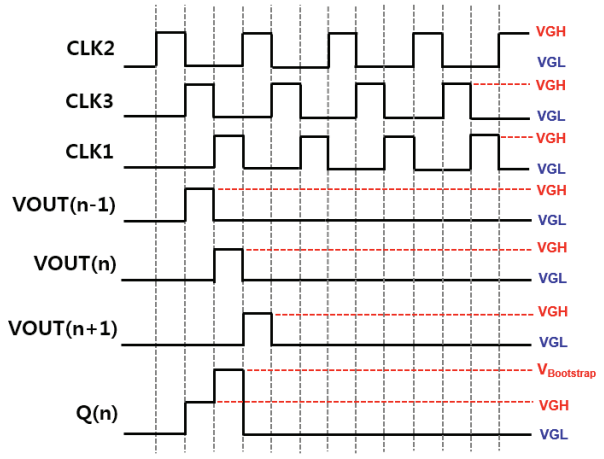
## 2 EXPERIMENT

In simulation, we set a-IGZO TFT model and designed a 11T1C new gate driver circuit based on a-IGZO TFTs as shown in Fig. 1 and Fig. 2 (a), respectively. Channel width and length of pull-down TFTs (T8, T9, and T10) are 150 μs and 5 μs respectively. We considered pull-down TFT is degraded due to the continuous gate bias stress, resulting in $V_{th}$ shift. Therefore, gate driver circuit is composed three pull down TFTs to reduce TFT degradation. Fig. 2 (b) exhibits a voltage waveform of the bus lines (CLK signals, VSS) and output signals. Operation sequences of proposed circuit are pre-charge period, bootstrapping period, and output discharging period as shown in Fig 2. First, gate voltage of T4 is pre-charged to +28 V. When Q node voltage is $V_{Bootstrap}$ through coupling of C1, output voltage maintains +28 V through pull-up TFT (T4) during 1H time. After this period, output voltage is continuously discharged through three pull down TFTs (T8, T9, and T10) using CLK signals. To realize proposed circuit in simulation, The $V_{th}$ of all TFTs

set to +3.5 V in proposed circuit. CLK signals, VOUT(n+1), and VOUT(n-1) swing from -5 V (VGL) to +28 V (VGH) and VSS is -5 V. 1H time is 7.7 μs considering full high definition (FHD, 1920x1080) and frame frequency of 120 Hz. More details are given in Table 1.




(a)




(b)

**Fig. 2 (a) Proposed gate driver circuit schematic and (b) Timing diagram**

**Table. 1 Device parameters of proposed circuit**

| Parameter | Value |
|---|---|
| T1-T11 L | 5 μm |
| T1, T3 W | 150 μm |
| T2 W | 100 μm |
| T4 W | 150 μm |
| T5 (Pull-up TFT) W | 250 μm |
| T6, T11 W | 120 μm |
| T8, T9, T10 (Pull-down TFT) W | 150 μm |
| T7 W | 150 μm |
| C1 | 1 pF |
| CLK1, CLK2, CLK3 voltage | -5 V to 28 V |
| CLK duty ratio | 33.3% |
| VSS | -5 V |
| CLK Frequency | 43.3 kHz |

**L: TFT channel length, W: TFT channel width**

## 3 RESULTS AND DISCUSSION

To reduce the ripples of output pulse, pull-down TFTs (T8, T9, and T10) are driven AC voltage with a duty ratio of 33.3% through CLK pulse instead of DC voltage driving. Gate voltage of pull-down transistors (T8, T9, and T10) is sequentially charged to +28 V for discharging of output voltage to -5 V since 23.1 μs as shown in Fig. 3. T10, T8, and T9 are continuously operated through CLK2, CLK3, and CLK1 respectively. Thus, ripple voltage of output is almost not generated because proposed circuit has 100% turn-off duty ratio. These operations can prevent degradation of pull-down TFT by continuous gate bias stress compared to DC-driven pull-down TFT. Besides, we simulated 1069$^{th}$, 1071$^{st}$, and 1073$^{rd}$ output pulse as shown in Fig. 4. Considering RC delay of gate line, a resistor of 5.6 kΩ and a capacitor of 139.4 pF were connected in parallel to the output node [13]. During 1H time, Output voltage of 1069$^{th}$, 1071$^{st}$, and 1073$^{rd}$ is saturated to +27.9 V, +27.89 V, and +27.89 V respectively. Based on the output voltage (+28 V), the error rate is 0.0036%, 0.0039%, and 0.0039% respectively. Therefore, output voltage of the proposed gate driver circuit successfully exhibited approximately +28 V about 1069$^{th}$, 1071$^{st}$, and 1073$^{rd}$ output voltage in simulation.

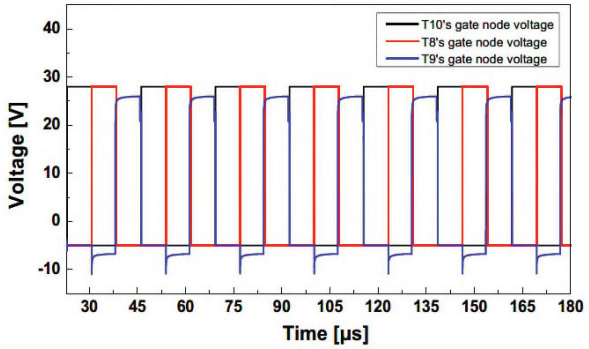



**Fig. 3 Voltage of gate node when T8, T9, and T10 are operated**

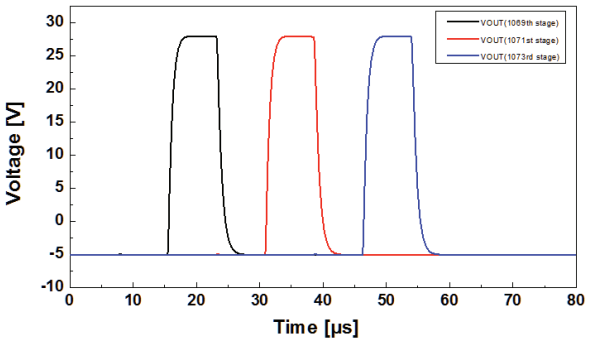



**Fig. 4 The simulated 1069$^{th}$, 1071$^{st}$, and 1073$^{rd}$ stage output pulse in proposed circuit**

## 4 CONCLUSIONS

In this paper, we proposed the 11T1C new gate driver circuit with three pull-down TFTs (T8, T9, and T10) based on a-IGZO TFTs for stable output node. Pull-down

transistors (T8, T9, and T10) are progressively operated to discharging of output voltage. We also researched about the simulated 1069th, 1071st, and 1073rd stage output pulse voltage in proposed circuit. Each of output voltage is +27.9 V, +27.89 V, and +27.89 V. Based on the output voltage (+28 V), the error rate is 0.0036%, 0.0039%, and 0.0039% respectively. In addition, ripple voltage of output node is not generated because proposed circuit has 100% turn-off duty ratio. Thus, a proposed gate driver circuit can be stably operated for output node voltage of all gate line.

**REFERENCES**


[1] E. Fukumoto, T. Arai, N. Morosawa, K. Tokunaga, Y. Terai, T. Fujimori, and T. Sasaoka, "High-mobility oxide TFT for circuit integration of AMOLEDs," *J. Soc. Inf. Disp.*, vol. 19, pp. 867-872, 2012.

[2] B. Kim, S. C. Choi, S-H. Kuk, Y. H. Jang, K-S. Pack, C. D. Kim, and M. K. Han, "A Novel Level Shifter Employing IGZO TFT," *IEEE Electron Dev. Lett.,* vol. 56, pp. 167-169, 2011.

[3] B. Kim, H. N. Cho, W. S. Choi, S. H. Kuk, Y. H. Jang, J. S. Yoo, S. Y. Yoon, M. C. Jun, Y. K. Hwang, and M. K. Han, "Highly Reliable Depletion-Mode a-IGZO TFT Gate Driver Circuits for High-Frequency Display Applications Under Light Illumination," *IEEE Electron Dev. Lett.,* vol. 33, pp. 528-530, 2012.

[4] K. N. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," *Nature,* vol.432, pp. 488-492, 2004.

[5] J. Y. Kwon, and J. K. Jeong, "Recent progress in high performance and reliable n-type transition metal oxide-based thin film transistors," *Semicond. Sci. Technol.,* vol.19, pp. 024002, 2015.

[6] D. H. Kim, H. J. Koo, M. G. Kang, K. I. Chun, U. H. Choi, Y. H. Ko, J. Y. J, C. Y. Jeong, Y. H. Jang, J. U. Bae, K. S. Park, S. Y. Yoon, and I. B. Kang, "Gate Driver Circuits for Internal Compensation Type OLED Display with High Mobility Oxide TFT", *J. Soc. Inf. Disp.*, vol. 49, pp 40-43, 2018.

[7] J. Oh, J.-H. Kim, K.-M. Jung, H. E. Kim, K.-R. Kim, K. Park, J.-H. Jeon, and Y.-S. Kim, "a-Si:H TFT-based gate driver circuit using Q node as both pull-up and hold-down controller," *Semicond. Sci. Technol.*, vol. 34, pp. 065014, 2019.

[8] K. Hoshino, D. Hong, H. Q. Chiang, and J. F. Wager, "Constant-Voltage-Bias Stress Testing of a-IGZO Thin-Film Transistors," *IEEE Trans. on Electron Dev.*, vol. 56, pp. 1365-1370, 2012.

[9] W.J. Wu, L. R. Zhang, Z. P. Xu, L. Zhou, H. Tao, J. H. Zou, M. Xu, L. Wang, and J. B. Peng, "A High-Reliability Gate Driver Integrated in Flexible AMOLED Display by IZO TFTs," *IEEE Trans. on Electron Dev.*, vol.64, pp. 1991-1996, 2017.

[10] J. W. Choi, M. S. Kwon, J. H. Koo, J. H. Park, S. H. Kim, D. H. Oh, S. W. Lee, and J. Jang, "Noble a-Si:H Gate Driver with High Stability," *J. Soc. Inf. Disp.*, vol.39, pp. 1227-1230, 2012.

[11] C.-L. Lin, C.-D. Tu, C.-E. Wu, C.-C. Hung, K.-J. Gan, and K.-W. Chou, "Low-power gate driver circuit for TFT-LCD application," *IEEE Trans on Electron Dev.*, vol. 59, pp. 1410-1415, 2012.

[12] K. Kurishima, T. Nabatame, T. Onaya, K. Tsukagoshi, A. Ohi, N. Ikeda, T. Nagata, and A. Ogura, "Suppression of threshold voltage shift on In-Si-O-C Thin-Film Transistor with an $Al_2O_3$ Passivation Layer under Negative and Positive Gate-Bias Stress," *IEEE EDTM*, vol. 9, pp. 74-76, 2019

[13] J.-H. Kim, J. Oh, K. Park, and Y.-S. Kim, "IGZO TFT gate driver circuit with large threshold voltage margin," *Displays*, vol. 53, pp. 1-7, 2018.