

Photo-induced instability behaviors of IGZO TFTs caused by the reversible charge trapping

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ABSTRACT

Photo-induced instability phenomena were investigated in IGZO TFT. The photo-responsivity behaviors attributed to the induced gate bias reveal that, resulting from their substantial trapping feature, photo-carriers (electrons and holes) activated in IGZO solid contribute differently to the negative shift V_{th} of the device. The bidirectional switching behavior under photo-irradiation also clearly indicates that the hysteresis enhancement predominantly comes from the long-lived reversible charge effect (holes) in n-type devices.

INTRODUCTION

For high performing the backplane units of flat-panel displays, amorphous indium-gallium-zinc-oxide (a-IGZO) transistor is a promising candidate to replace amorphous silicon (a-Si:H), currently the most popularly used thin-film device in the backplane system, as its field effect mobility is of a magnitude dozens of times higher than that of the a-Si:H device [1]. Their processes compatible with the conventional backplane processing as well as at low-temperatures also indicate that a-IGZO devices might be one of the most suitable backplane devices to obtain the high performance electronics on plastic [2].

However, despite enormous progress in improving its electrical performance, the devices based on metal-oxide semiconductor show crucial instability of the threshold voltage shift (ΔV_{th}) or hysteresis, brought about by bias stress, which also become worse by environment effect such as illumination or humidity etc. [3, 4]. These facts emphasize the importance of clarifying the relationship between the electrical properties of metal-oxide devices and environmental factors to achieve a highly stable backplane as a reliable function of electronics applications.

In this work, we describe our findings in understanding and characterizing the photo-responsible feature of a-IGZO TFTs. Electro-optical analysis demonstrates that the device instability phenomena caused by the role of the reversible carriers excited by the incident photon; it shows the substantial bias-induced ΔV_{th} feature under photo-irradiation governed by the positive charge (hole) trapping, presenting the possible mechanism of ΔV_{th} under photo-irradiation. The hysteresis responses for the incident photo also allowed us to identify that enhanced hysteresis behaviors would be associated with captured holes in localized state and their long-lived feature in the forbidden gap states of IGZO.

EXPERIMENT

The a-IGZO transistors and their backplane array were fabricated with a bottom gate and top S/D geometry on the carrier glass substrate. The schematic of the device is presented as a cross-sectional view in Fig. 1. A 530-nm-thick copper (Cu)/Molybdenum (Mo) was deposited by DC sputtering for the gate metal. A 400 nm thick silicon nitride (SiNx)/silicon dioxide (SiO₂) bi-layer as a gate dielectric was formed by plasma enhanced chemical vapor deposition (PECVD). IGZO with a In₂O₃:Ga₂O₃:ZnO= 1:1:1 mol% ratio was deposited through direct-current (DC) sputtering at a total thickness of 60 nm at room temperature (RT) to form an a-IGZO active layer, and then it was patterned via photolithography. Cu/Mo with 530 nm thickness was deposited on active layer, and was patterned to form an S/D electrode employing an etch-back process. The passivation layers (PAS) of SiNx/SiO₂ was deposited consequently by PECVD and via holes were formed. As the final step, a 75-nm-thick indium-tin-oxide (ITO) pixel electrode was deposited, and the anode was defined. The TFTs completed with the channel-width-to-length ratio (W/L) of 10/5-10/50 μm in the array.

The device characteristics were examined in the dark or under a light at room temperature. The light was provided by a xenon lamp and the visible-light spectrum was prepared with a wavelength in the range of 400–800 nm through a band pass filter, which illuminated from above on to the device as shown in Fig. 1(right). The intensity of the light was set at 22.4 mW/cm² and it is modulated as the different intensities by controlling light power. The current-voltage (I-V) characteristics were examined with a Keithley 4200-SCS semiconductor parameter analyzer. An Inspection in the device structure was carried out via focused ion beam scanning electron microscopy (FIB-SEM).

RESULTS

Fig. 2 shows the device features in the dark and under visible light illumination. The devices were examined at the gate bias sweeping from -20 to +20 V with the source-drain bias (V_{DS}) of 1.0 V under a modulated light power of 5, 15, 30 and 60%. In the dark, the transfer characteristics of the device show the typical current-voltage (I-V) behavior of n-channel FETs with low off-current (I_{off}) feature close to 10⁻¹³ A. Under photo-irradiation, the linear plot of drain current (I_D) versus

gate–source voltage (V_{GS}) clearly presents the noticeable photo-response feature as the increase in I_{off} level and ΔV_{th} shift into the negative direction. It was thought that the widely observed current enhancement under light might arise from the increase in the photoexcited majority carrier after electron–hole pair generation in the channel of the metal-oxide device under photo-irradiation [5].

Figure 3 shows the device stability features relying on bias sweep direction and ambient condition. In the dark, when the applied bi-directional bias was applied from the forward to the reverse bias, only slight “anti-clockwise” hysteresis loops was found towards a negative direction as shown in Fig. 3. This is the comparable with that of previous reports in IGZO devices [6]. In comparison with that result, Figure 3 also shows that the present device strongly response regarding to the integrity feature in the case where the device is exposed to photo-irradiation. Distinct hysteresis with the negative shifts in V_{th} are observed in the reverse sweep, especially when the device is biased up to the depletion (negative) regime. The off current level is also proportionally enhanced by increasing the incident VIS power in the negative bias. Here, it is also noteworthy that ΔV_{th} shows the similar values in enhanced hysteresis under VIS light even the incident light power was modulated from 5 to 30 %.

To understand that photo-induced instability kinetic in metal-oxide device, the device characteristics are functionalized by the various bias sweeps and the photo-irradiation. Figure 4(left) presents the I–V characteristics and V_{th} when the device is swept at the different gate biases from -20 to $+20$ V with the interval of 5 V in the dark. Typical n-channel FET transfer characteristic was clearly observed with low I_{off} feature. It is also obviously found that the I–V characteristics of V_{th} in the dark are independent of the starting voltage of each bias sweep. In comparison with that result, Figure 4(right) shows different I–V behaviors in the case where the device is exposed to photo-irradiation. Similar I–V characteristics are obtained when the starting voltage is set at different accumulation (positive) biases for the n-channel device. However, the device exhibits a photoresponse feature under the case that a depletion (negative) bias is set as the onset voltage. The threshold voltage of about 3 V was shifted in a negative direction when the device was swept from the gate bias of -20 V under photo-illumination. More photoresponse behaviors of the V_{th} result from when the onset voltage was set with the negative biases as shown in Fig. 4(b). The threshold voltage is proportionally shifted by increasing the induced starting voltage in a negative direction under photo-irradiation.

Here, it is also noteworthy that the subthreshold slope (SS) characteristic of the device is continually degraded when the device is driven toward the negative bias under light. It reveals that V_{th} behavior would be predominantly attributed to the charging and discharging process of the

carriers in the interfacial region than that in the bulk of the active region.

These V_{th} responses, characterized by the bias and the photo-irradiation, allow us to understand that the mechanism of the change in the threshold voltage in energy space is derived from charge capturing. Figure 5 shows schematic energy-band diagrams explaining the bias dependence of V_{th} caused by the hole tapping feature only observed under the photo-irradiated condition. When the device is set in the dark, the minority carrier (hole) injection into the channel would be restricted due to the high-energy barrier ($q\phi_B$) between the valence band (E_v) level in active layer and the metal electrodes. Therefore, only unipolar carriers (electrons) would be expected to have a role as the carrier transport and in trapping. In the case where the trap states for electrons are uniformly distributed in the gap state, the given bias would cause I–V characteristics similar to that of the n-type device as an independent function of the onset voltage [Fig. 5(left)]. However, the photo-irradiation of the device with energy exceeding the optical band gap of IGZO leads to the generation of a number of excess free carriers. If the device is set with a depletion gate bias, the excited holes are occupied in the localized trap state, which contributes to an decrease in the surface potential, causing the threshold voltage shift of the device to move in a negative direction, as is only observed under lighted conditions [Fig. 5(right)]. Here, the negative V_{th} would be accelerated by increasing the depletion gate bias, owing to the fact that more charges are involved in deeper energy states in the forbidden gap of active region as is observed in Fig. 5(right). This result also clearly addresses the situation in which a number of hole trap sites are localized in the IGZO gap state, playing a significant role in the device instability.

The electrical characteristics relying on the bi-directional bias sweeps are presented in Fig. 6, which helps to understand the properties of trapped charges causing instability variation under light. The device was swept as the sets of the gate biases of $0 \sim -20 \sim 0$, $0 \sim -15 \sim 0$, $0 \sim -10 \sim 0$, and $0 \sim -5 \sim 0$ in the dark and under VIS light condition. As shown in Fig. 6(right), the hysteresis characteristics of the device with bi-directional bias sweeps in the dark are independent of the starting voltage of each bias sweep. Namely, almost the same current–voltage (I–V) characteristics with the virgin sweep were obtained even if the sweeping bias was set at different reverse (negative) voltages for the n-channel device. On the other hand, as shown in Fig. 6(left), threshold voltages about -3 , -4 , -6 and -8 V are observed in the reverse sweep when the device is swept from the reverse biases of -5 , -10 , -15 , and -20 V under light, respectively. The hysteresis is also enhanced with the increase of the sweeping voltage toward the negative direction.

The movement of hysteresis in a negative direction only observed under photo-irradiation indicates the contribution of trapped holes, and shows the detrapping kinetic of them. That is, in the case that the device is set with the depletion bias under incident light with energy higher than the forbidden gap of active layer leads to the generation of the excess holes and their occupation in the localized trapping states with causing the positive V_{th} shift as we discussed earlier [Fig. 7(left)]. Here the charge capturing in the deeper energy states at the interface is increased by increasing the reverse bias. When the gate bias is set at the onset voltage of the device [Fig. 7(right)], the hole trapping is prevented and some trapped holes are detrapped due to the opposite field at the interface. Furthermore, the negative bias induced electrons may lead to the recombination of trapped holes at the interface.

Here, it is also found that hysteresis is enhanced in proportional to increase reverse sweeping biases, V_{th} also is not fully recovered to the initial condition according to higher negative-bias sweeps. Since the higher depletion bias would give rise to the hole trap further involving the deeper level with increasing hysteresis, this reflects that captured holes in the deep state would be associated with the slow detrapping process arising from the long-lived feature of holes. This result also shows that possible memory operation in metal-oxide device such as the photo chargeable memory device using the trap-and-release process.

DISCUSSION

A systematic investigation carried out for understanding and characterizing the photo-responsive stability in a-IGZO TFTs. Here, the electro-optical analysis shows that the device instability phenomena is caused by the role of the reversible carriers, excited by the incident photon; it shows the substantial bias-induced ΔV_{th} feature under photo-irradiation governed by the positive charge (hole) trapping, presenting the possible mechanism of ΔV_{th} under light. The hysteresis responses for the incident photo also allowed us to identify that enhanced hysteresis behaviors would be associated with captured holes in localized state and their long-lived feature in the forbidden gap states of IGZO.

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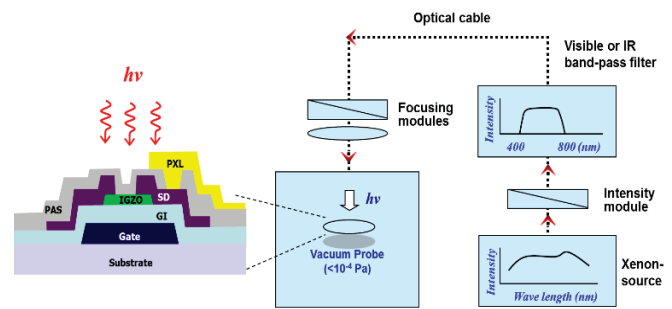


FIG.1 Device structure of a-IGZO transistors fabricated with a bottom gate and top S/D geometry. Schematic of photo-irradiation measurement for illuminating on the device

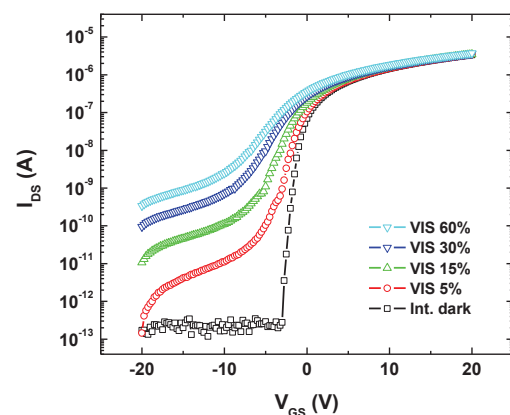


FIG.2 Transfer characteristics of the device ($W/L = 10 \mu\text{m}/5 \mu\text{m}$) as a function of incident light intensity. The light intensity was modulated from 5% to 60% at fixed light source intensity of $22.4 \text{ mW}/\text{cm}^2$

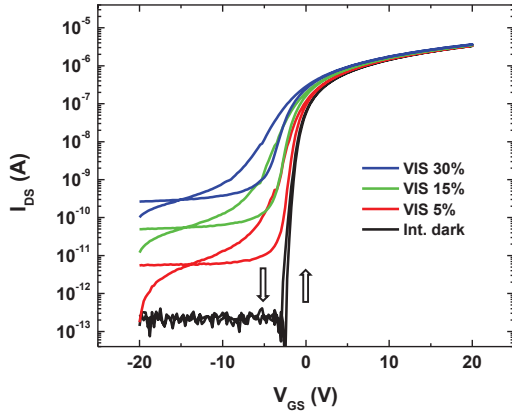


FIG.3 Hysteresis characteristics relying on ambient conditions (in the dark and under light irradiation). The device was measured at a fixed drain bias of 1V under the bidirectional gate bias sweeps: forward ($-20 \sim +20 \text{ V}$) and reverse ($+20 \sim -20 \text{ V}$).

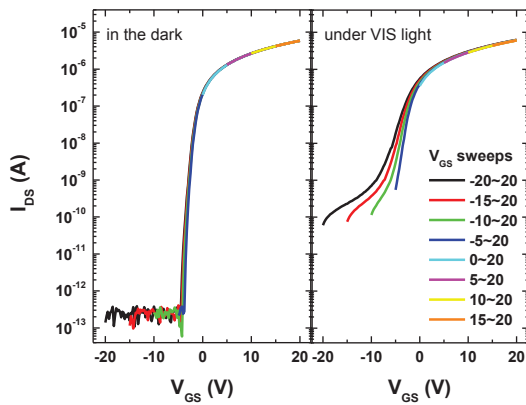


FIG.4 I-V characteristics as a function of different gate biases and incident light; The gate bias sweeping from -20 to $+20$ with the interval of starting gate bias of 5 V (left) in the dark and (right) under light irradiation

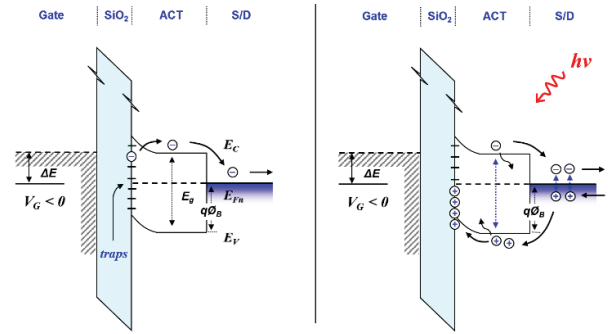


FIG.5 Model of energy-band diagrams for charge trapping with different ambient; (left) $V_G < 0 \text{ V}$ in the dark, and (right) $V_G < 0$ under light with energy higher than the optical band gap of IGZO. Note that, $V_G = 0$ does not mean the flat-band condition.

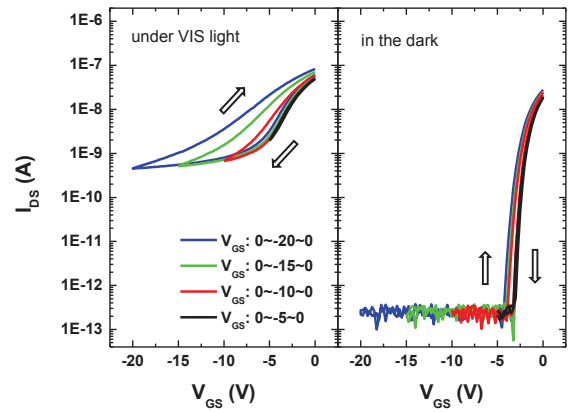


FIG.6 ΔV_T and hysteresis characteristics as a function of different ambient and biases; (left) depletion biases sweep under light (right) depletion biases sweep in the dark. Transfer characteristics were measured at a fixed drain bias of 1 V

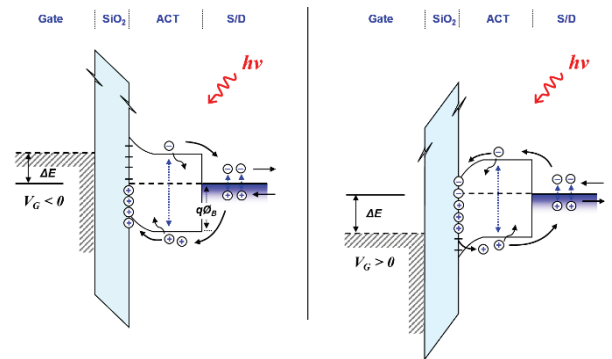


FIG.7 Schematic of energy-band diagrams for (left) the ΔV_T assigned by the charge capturing in relation to optical excitation as shown in the right Fig. 5 and (right) discharging process of trapped carriers