Self-Heating Effect of Low-Temperature Polycrystalline Silicon Thin Film Transistor Considering Grain Boundary Protrusion

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ABSTRACT

A proper estimation of the self-heating effect is crucial to ensure the reliable performance of high mobility transistors. We perform Silvaco TCAD based thermal distribution modeling in grain, grain boundary (GB) and protrusion of excimer laser annealed (ELA) low-temperature polycrystalline (LTPS) silicon thin-film transistors (TFTs).

1 INTRODUCTION

Performance deterioration in semiconductor devices due to self-heating phenomena is a serious issue to overcome for achieving highly reliable and efficient electronic systems. For high mobility transistors, this problem is even more pronounced. Among thin-film transistors (TFTs), low-temperature polysilicon (LTPS) TFTs has considered as one of the best choices for next-generation active-matrix organic light-emitting diode (AMOLED) based displays and driving circuits because of its high mobility and stability [1-3]. In contrast, p-channel LTPS TFTs are preferred over n-channel LTPS TFTs because of less likely to be influenced by hot carrier effect [4-5]. However, p-channel LTPS TFTs suffer from considerable electrical degradation while operating at high bias and temperature [6].

Despite many advantages of excimer laser annealed (ELA) LTPS TFTs, smaller grain size (100~500 nm), complex process flow, GB protrusion, aggressive fabrication cost are regarded as the main issues to overcome [7-9]. However, there are few reports addressing the self-heating problem in LTPS TFTs even though it causes significant degradation in electrical characteristics under the high gate and drain bias [10-12]. None of the reports discussed the thermal distribution extensively in the GB and GB protrusion of the polycrystalline silicon region. In our previous work, we demonstrated a detailed analysis of the effect of GB protrusion on the electrical characteristics in LTPS TFTs, which leads us to study thermal distribution in GB and GB protrusion [13].

In this report, we performed a detailed thermal distribution analysis in polysilicon grain, GB, and GB protrusion under high drain and gate bias by TCAD. Prior to temperature simulation, transfer and output characteristics are well fitted with measured data by the density of state (DOS) model. Temperature contour mapping reveals a clear indication of considerably high joule heating at the edges and peaks of the GB protrusions compared to the center of GB protrusion which may help to understand the bias induced thermal instabilities in LTPS TFTs.

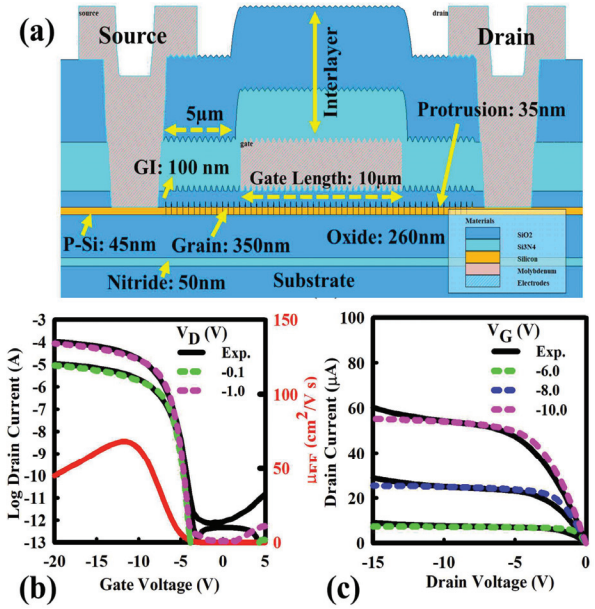

Figure 1: (a) TCAD generated schematic cross-sectional view of LTPS TFT with detailed device dimension, (b)-(c) transfer and output characteristics of the fabricated TFTs. Solid lines are experimental data and dashed lines are TCAD fitting.

2 EXPERIMENT

Fig.1 (a) shows the two-dimensional (2D) cross-sectional view of the fabricated LTPS TFT with ~350 nm grain, ~1 nm GB and 35 nm tall GB protrusion [13]. The p-channel coplanar LTPS TFT as depicted in Fig. 1(a) was fabricated on a glass substrate. A stacked layer of SiNx (50 nm) and SiOx (260 nm) was deposited by plasma-enhanced chemical vapor deposition (PECVD) at 450°C as a buffer layer. A 45 nm thick a-Si layer was deposited by PECVD at 420°C, followed by a dehydrogenation process. Excimer laser annealing (ELA) was performed to crystallize the a-Si layer and subsequently patterned to form active-island. A 100 nm thick SiOx by PECVD and 300 nm thick Cr by physical vapor deposition (PVD) were deposited, as gate insulator and electrode respectively. Source/drain (S/D) regions were P+ implanted and vacuum annealed at 360°C to activate the dopant. Next, 300 nm thick SiOx and 300 nm thick SiNx stacked-layer were deposited at 360°C as interlayer dielectric, followed by via hole formation for S/D contacts. Finally, a 250 nm thick Cr

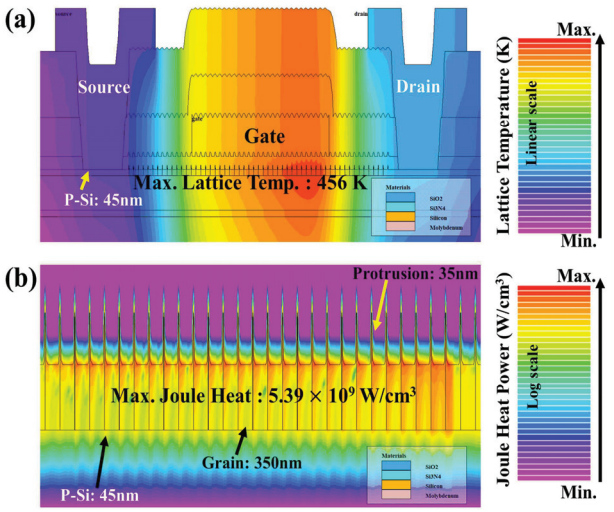

Figure 2: (a) Cross-sectional view of lattice heating profile that exhibits a maximum lattice temperature of 456 K, **(b)** distributed Joule heating power in the active region of the p-channel LTPS TFT with maximum Joule heat power of 5.39×10^9 W/cm^3 at the edge of GB and GB protrusion.

layer was deposited by PVD for S/D electrodes and vacuum annealed at 425°C for an hour to thermally activate the device.

The fabricated TFT has the channel width/length (W/L) of 40 µm/ 10 µm, respectively. The electrical characteristics of the fabricated LTPS TFTs were measured using an Agilent 4156C semiconductor parameter analyzer. Prior to thermal simulation, measured electrical characteristics were well fitted using Silvaco TCAD. Two different density of states (DOS) models were used to fit the data in order to achieve an accurate thermal model. All thermal simulation was performed considering a high gate and drain bias of -15 V and -10 V respectively.

3 RESULTS AND DISCUSSION

Fig. 1(b) and (c) demonstrate the transfer and output characteristics of the fabricated ELA LTPS TFT. A well-matched TCAD simulated transfer and output characteristics support the validity of the DOS model along with good accuracy of the thermal simulation. The lattice heating profile of the simulated device is shown in Fig. 2(a) for a given gate and drain bias of -15 V and -10 V respectively.

The distributed lattice temperature profile indicates that the center part of the TFT experience a relatively high temperature compared to the rest of the device. A maximum lattice temperature of 456 K is observed at the centermost drain side of the device which clarifies that the TFT might be overheated under high drain and gate bias.

Performance degradation due to high-current is commonly known as self-heating or Joule heating phenomenon and is a severe problem in polycrystalline devices [10] which is clearly visible in Fig. 2(b). As we consider the GB and GB protrusion in the simulation, it is now quite obvious that Joule heat dissipation uniformity has a strong dependency on the number of grain, GB and GB protrusion. With increasing the number of grain as well as GB, the heat dissipation in the active layer

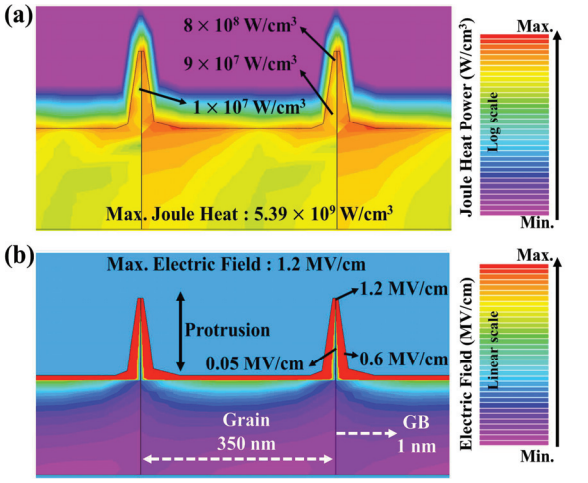

Figure 3: (a)-(b) Zoom-in distribution of Joul heat power and electric field at poly-Si grain, GB and protrusion.

becomes more discrete. A higher number of poly-Si grains or in another word, the small size of grain makes the number of GB protrusion higher and thus it makes the Si/SiO_2 interface more vulnerable under high bias stress. A maximum Joule heat power of 5.39×10^9 W/cm^3 is calculated at the edge of GB and GB protrusion using TCAD simulation, possibly this can accelerate the rate of defect creation at the interface.

Fig. 3(a) shows the Joule heating contour mapping within the grain boundary protrusion where the maximum Joule heat is dissipated at the edges of the protrusion. Joule heat power at top edge, center and bottom edge are 8.0×10^8 W/cm^3, 1.0×10^7 W/cm^3, and 9.0×10^8 W/cm^3, respectively. In contrast, each protrusion creates an arc-like distribution towards the gate insulator region. Higher the length of the protrusion, the more it will affect the gate insulator and consequently lead to even more pronounced thermal instability by introducing gate leakage and defects at the interface region. The length of the protrusion also has an impact on overall electrical deterioration as it changes the interface length. However, in this study the length of the protrusion considered is 35 nm which determined by transmission electron microscopy (TEM), detail information can be found in our previous study [13].

To support the claim of Joule heat distribution within the protrusion, electric field contour mapping is also shown in Fig. 3(b). However, a similar arc-like pattern is observed which suggests that the electric field is highly concentrated at the edges and minimum at the center of the GB protrusion. The electric field at the center and the edges of the protrusion are 1.2 MV/cm and 0.6 MV/cm, respectively. This electric field distribution also reveals that electron concentration at the center of the protrusion is minimum which one is of the major findings of our previous work [13].

Fig. 4(a) represents the plot of the electric field and dissipated Joule heat power based on the cutline shown in Fig. 4(c) to observe the relationship between these two. The cutline includes the edges of grain, GB and GB protrusion bottom edge. Fig. 4(a) indicates that the electric field is much higher

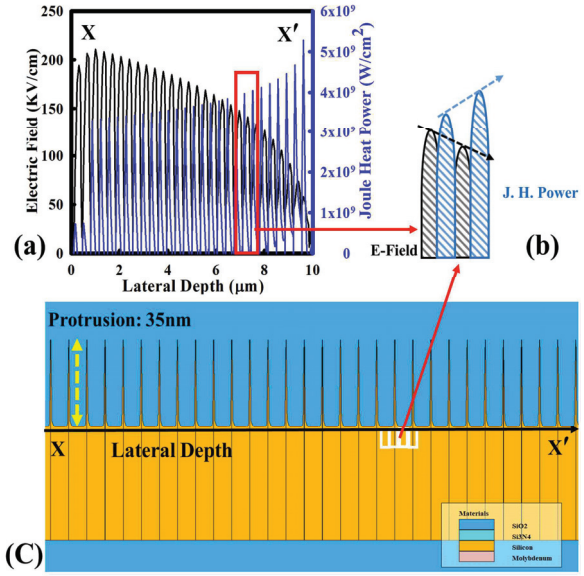

Figure 4: (a) Electric field and Joule heat power depth profile using the lateral depth cutline (XX′) as shown in Fig. 4(c). (b) At a given point on the cutline, resistive power is high for a weak electric field and vice-versa. (c) Considered cutline in SILVACO ATLAS generated structure file to analyze the parameters.

between consecutive protrusions as compared to the GB and GB protrusion bottom edges because the applied potential can directly cut them. On the other hand, bottom edges of the protrusions show weaker field distribution as electric filed is preoccupied by the top edges of the protrusion. The comparatively weaker electric field of these regions accumulates significantly lower hole concentration and thus high resistive behavior, which is the reason for resistive heating that might be more pronounced in these regions. In addition to that, throughout the cutline the electric field and Joule heat dissipation show the opposite relationship to each other as electric filed is proportionally related to current and voltage. An elaborated figure of this phenomenon of Fig. 4(a) is displayed in Fig. 4(b). Inclusively, an explicit non-uniform heat dissipation mapping is perceived through this thermal analysis because of including GB and GB protrusion which may help to understand some effects like anomalous humps, kink effect, and degradation during NBTS [14-15].

4 CONCLUSIONS

We analyze the thermal performance of the P-type LTPS TFT under high gate and drain bias considering measured poly-Si grain, GB and GB protrusion. Simulation results suggest that GB and GB protrusion have significant impact on device thermal performance. Joule heating under high gate and drain bias exhibits non-uniform thermal distribution in active layer due to GB and GB protrusion. This study may help to understand the critical thermal instabilities due to self-heating and thus an improved design can be accomplished to overcome these issues.

REFERENCES

[1] M. Stewart, R. S. Howell, L. Pires and M. K. Hatalis, "Polysilicon TFT technology for active matrix OLED displays," in *IEEE Transactions on Electron Devices*, vol. 48, no. 5, pp. 845-851, May 2001. doi: 10.1109/16.918227.

[2] M. Kimura *et al.*, "Low-temperature polysilicon thin-film transistor driving with integrated driver for high-resolution light emitting polymer display," in *IEEE Transactions on Electron Devices*, vol. 46, no. 12, pp. 2282-2288, Dec. 1999. doi: 10.1109/16.808054.

[3] C. Fan, Y. Chen, C. Yang, Y. Tsai and B. Huang, "Novel LTPS-TFT Pixel Circuit with OLED Luminance Compensation for 3D AMOLED Displays," in *Journal of Display Technology*, vol. 12, no.5, pp. 425-428, May 2016. doi: 10.1109/JDT.2016.2525736.

[4] L. Mariucci, A. Valletta, P. Gaucci, and G. Fortunato, "Hot-carrier effects in p-channel polycrystalline silicon thin film transistors," *Appl. Phys. Lett.*, vol. 89, no. 18, p. 183 518, Oct. 2006. doi: 10.1063/1.2378587.

[5] Y. Uraoka, Y. Morita, H. Yano, T. Hatayama, and T. Fuyuki, "Gate length dependence of hot carrier reliability in low-temperature polycrystalline-silicon P-channel thin film transistors," *Jpn. J. Appl. Phys.*, vol. 41, pp. 5894–5899, Oct. 2002. doi: 10.1143/JJAP.41.5894

[6] S. Hashimoto, Y. Uraoka, T. Fuyuki, and Y. Morita, "Analysis of thermal distribution in low-temperature polycrystalline silicon p-channel thin film transistors," *Jpn. J. Appl. Phys.*, vol. 45, no. 1A, pp. 7–12, 2006. doi: 10.1143/JJAP.45.7.

[7] D. K. Fork, G. B. Anderson, J. B. Boyce, R. I. Johnson, and P. Mei, "Capillary waves in pulsed excimer laser crystallized amorphous silicon," *Appl. Phys. Lett.*, vol. 68, no. 15, pp. 2138–2140, Apr. 1996. doi: 10.1063/1.115610.

[8] T. Sameshima, S. Usui, and M. Sekiya, "XeCl excimer laser annealing used in the fabrication of poly-Si TFT's," *IEEE Electron Device Lett.*, vol. 7, no. 5, pp. 276–278, May 1986. doi: 10.1109/EDL.1986.26372.

[9] M.-K. Kang, S. J. Kim, and H. J. Kim, "Fabrication of high performance thin-film transistors via pressure-induced nucleation," *Sci. Rep.*, vol. 4, Oct. 2014, Art. no. 6858. doi: 10.1038/srep06858.

[10] G. Fortunato, M. Cuscuna, P. Gaucci, L. Maiolo, L. Mariucci, A. Pecora, A. Valletta, and F. Templier, "Self-heating effects in p-channel polysilicon TFTs fabricated on different substrates," *J. Korean Phys. Soc.*, vol. 54, no. 925, pp. 455–462, Jan. 2009. doi: 10.3938/jkps.54.455.

[11] P. Gaucci, A. Valletta, L. Mariucci, A. Pecora, L. Maiolo and G. Fortunato, "Analysis of Self-Heating-Related Instability in Self-Aligned p-Channel Polycrystalline-Silicon Thin-Film Transistors," in *IEEE Electron Device Letters*, vol. 31, no. 8, pp. 830-832, Aug. 2010. doi: 10.1109/LED.2010.2051137.

[12] B. Chen *et al.*, "Systematic Analysis of High-Current Effects in Flexible Polycrystalline-Silicon Transistors Fabricated on Polyimide," in *IEEE Transactions on Electron Devices*, vol. 64, no. 8, pp. 3167-3173, Aug. 2017. doi: 10.1109/TED.2017.2715500.

[13] M. M. Billah *et al.*, "Effect of Grain Boundary Protrusion on Electrical Performance of Low Temperature Polycrystalline Silicon Thin Film Transistors," in *IEEE Journal of the Electron Devices Society*, vol. 7, pp. 503-511, 2019. doi: 10.1109/JEDS.2019.2911088.

[14] K. W. Kim, J. Kang, H. Ku, K. Lee and H. J. Kim, "Anomalous Kink Effect Induced by Bottom-Shield-Metal in LTPS TFTs on Plastic Substrates," in IEEE Electron Device Letters, vol. 39, no. 10, pp. 1524-1527, Oct. 2018. doi: 10.1109/LED.2018.2867942.

[15] H. Chen et al., "A Novel Heat Dissipation Structure for Inhibiting Hydrogen Diffusion in Top-Gate a-InGaZnO TFTs," in IEEE Electron Device Letters. doi: 10.1109/LED.2019.2927422