Analysis of Horizontal-Mura Caused by Reset's Abnormal Delay of GOA Output

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ABSTRACT

A rare failure named Horizontal-Mura caused by reset's abnormal delay of GOA output is studied systemically. By increasing frame frequency, changing TFT size ratio and increasing channel Length, the leakage current of voltage Gout's Gate (PU) can be reduced, and Mura phenomenon can be significantly alleviated.

1 INTRODUCTION

TFT-LCD is widely used in display, where GOA (Gate Driver on Array) is the current mainstream with the advantages of narrow border and low cost [1~3]. GOA is based on the control signal provided by the external circuit (CLK, Input and VDD Signal), and fabricated with the same process of TFT [4~5]. Horizontal-Mura is a kind of Mura which is obviously related to the design of GOA. In this paper, the mechanism and influencing factors of this phenomenon are analyzed thoroughly. The excessive leakage current of GOA's TFT is the main reason of the Gout's abnormal reset.

2 Horizontal-Mura

As shown in Figure 1, the phenomenon of Horizontal Mura is along the Gate direction, where other colors pixel (blue and red) shine as green pixel does in green picture. This phenomenon changes with frame frequency and VGH (the highest voltage of signals (CLK, Input, VDD) provided by external circuits). And there are significant differences in severity of Horizontal-Mura in different area.

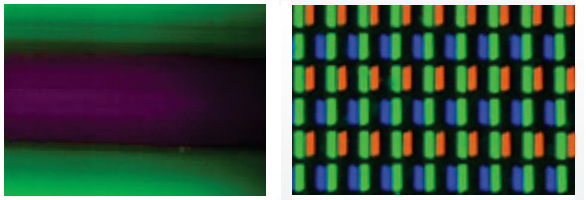


Fig. 1 Horizontal-Mura and micrograph

The pixels arrangement, sequential voltages (Gate and Data), GOA (12T1C, 12 Transistors/1 capacitor) Model and the waveforms of GOA signal are figured out as Fig.2~Fig.4 for describing the mechanism of this phenomenon.

As shown in Figure 2, pixels are arranged in Z-Inversion structure, and the adjacent Data's polarities are opposite. In green picture, the blue pixel (Gate 1, Data 2) is possible to be mischarged when green pixels (Gate 2, Data 2) is charging. The time difference setting between the falling edge of Gate signal and the rising edge of Data signal is named T_{GOE}. When Gout delay T_F (Time Fall: 90% -> 10%) is longer than T_{GOE}, the crosstalk of Data signal will happen, and the longer the T_F, the more charge of blue pixel, which induces the Horizontal-Mura more obvious.

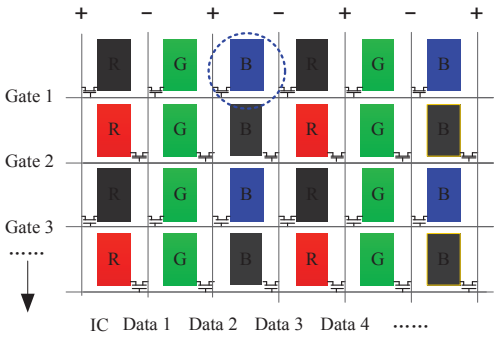


Fig. 2 (a) Pixel Arrangement

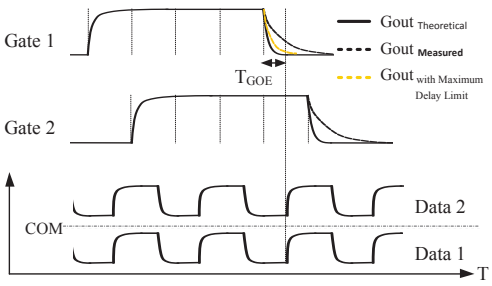


Fig. 2 (b) Sequential Voltages of Gate and Data

Figure 3 is the GOA (12T1C) model. PU carry unit is T1 and PU reset unit is T2. PU denoise units are T9/T8, T5/T6 and T10, Gout output unit is T3, and Gout noise reduction unit is T11. Because the reset of Gout follows CLK signal and there is no other active reset TFT for Gout, the stability of T3's gate voltage (PU) is the key to ensure the normal reset of Gout.

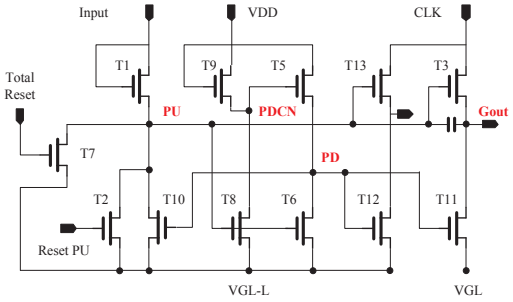


Fig. 3 GOA 12T1C Model

Figure 4 is the waveform of Gate, PU, PD and PDCN when GOA works. In the period 1, when Input is in carry, PU rises to a high level, Gout and CLK are connected; In the Period 2, when CLK enters a high level, the bootstrap voltage of PU is further increased because of capacitance C; In the Period 3, Gate decreases to a low level (VGL) with CLK; and the PU at the Period 3 ending is reset to a low level. When PU is high, PD and PDCNs are in low level theoretically. If the leakage of PU increase, the voltage in the Period 3 would decrease (the dotted line), and the Gout reset delay T_F would increase, which would cause Data signal crosstalk.

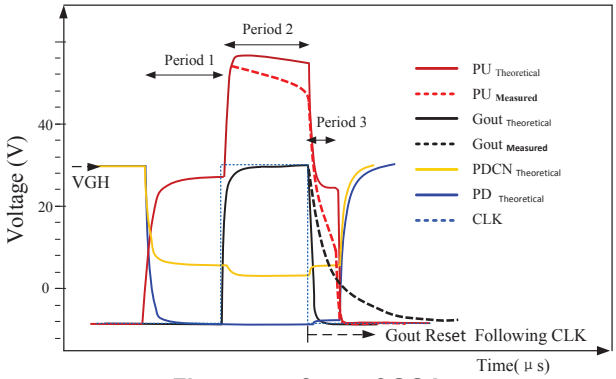
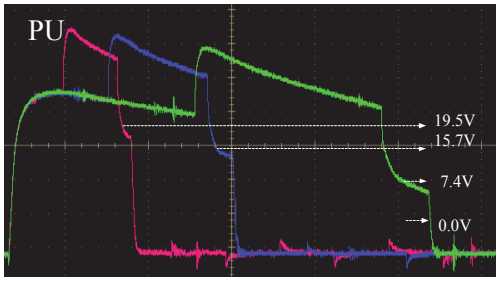


Fig. 4 waveform of GOA

3 Influence Factors of Horizontal-Mura

3.1 Frequency

Horizontal-Mura becomes more serious with the decrease of frame frequency. Figure 5 shows the PU and Gout waveforms in Mura region at the frequencies of 165Hz, 90Hz and 48Hz when VGH is 36V. It can be seen from the slope of voltage drop in the Period 2 of PU that the decreasing speeds of PU voltage at different frequencies are the same with time, and the smaller the frequency (the longer the leakage time corresponds to), the greater the decrease of PU voltage (19.5V, 15.7V and 7.4V respectively at the Period 3 ending). The corresponding Gout reset delay T_F are 5.0, 8.2 and 10.7 us, respectively. When PU voltage drops to 7.4V, T3 is not fully turned on, and Gout voltage cannot be reset with the decrease of CLK in time.



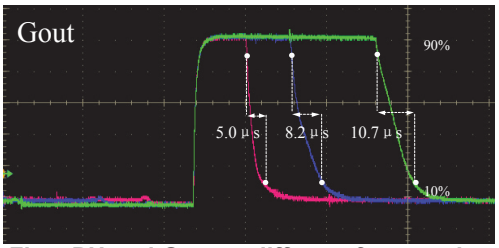


Fig.5 PU and Gout at different frequencies

3.2 TFT Ratio

T2, T10 and T7 are closed when PU is at high voltage level ideally. Actually, the leakage current cannot be neglected. Taking T10 as an example, as shown in Figure 6, the channel number is reduced by laser cutting, and T10 can be cut down to 2/5 under normal display conditions (-20 ℃ ~ 60 ℃). After 3/5 cut, Mura phenomenon at the cutting position was significantly alleviated. As shown in Figure 7, PU and Gout are measured before and after cutting (Frequency 48Hz and VGH 36V). Before cutting, the voltage of PU is 10.6V at the Period 3 ending. After T10 cut 3/5, the voltage rises to 19.7V, and the corresponding Gout reset delay decreases from 7.5 to 3.9 us.

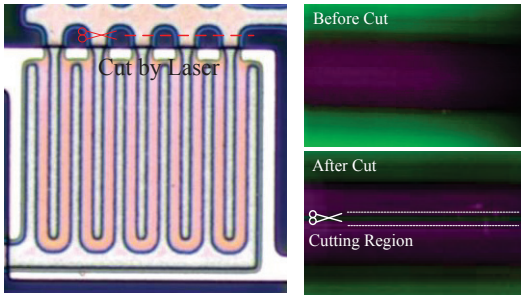


Fig. 6 T10 cut by laser

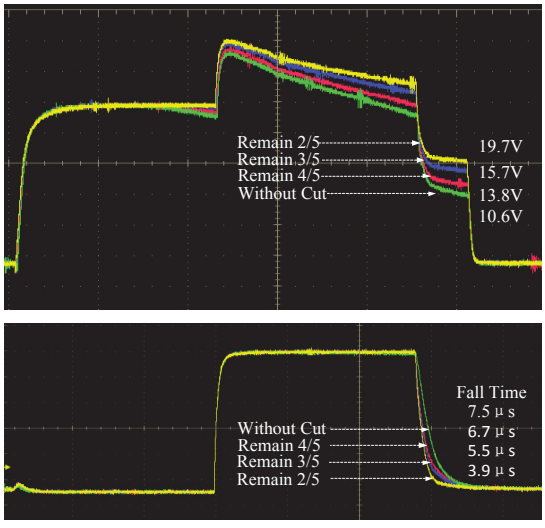


Fig. 7 PU and Gout changes with T10 cut

The ratio of TFT with different functions is obtained by simulation, and the theoretical redundancy of VGH is

large. As shown in Figure 8, when VGH increases (30V-> 40V), the PU voltage at the Period 3 ending decreases rapidly (9.7V-> 2.0V), which makes the Gout output reset abnormally. The change of Vds and Vgs with the increase of VGH is not the main reason of the increase of T10's leakage current, for PU at the beginning of the Period 3 is almost unchanged. As shown in the figure 8, the voltage of PD and PDCNs is measured: when their voltages rise, the gate voltage of T10 increases, which makes the PU voltage drop rapidly.

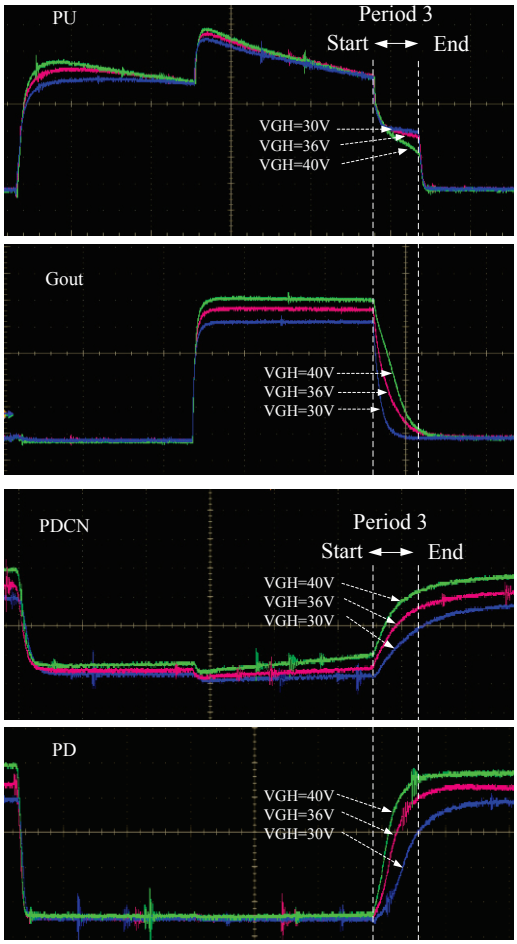


Fig. 8 Gout, PU, PDCN and PD Changes with VGH

Usually, changes of VGH (30V~40V) will not cause significant changes in PDCN and PD. However, when PU is at a high level, and the large proportion of noise reduction unit T9/T8 and T5/T6 will lead to: the discharge efficiency of VGL for PDCN is less than the charge efficiency of VDD for PDCN; at the same time, the discharge efficiency of VGL for PD is less than the charge efficiency of PDCN for PD, which will increase the voltage of PDCN and PD. With VGH rises, the conductivity of T9, T8, T5 and T6 increase, and the efficiency difference between charge and discharge increases. After the number of channels in T9 and T5 gradually reduced by laser cutting, Mura's phenomenon became slighter. Therefore, when VGH increases, the larger ratio of TFT T9/T8 and T5/T6 is the reason for the decrease of PU voltage.

The leakage of PU can also pass through T2 and T7. Table 1 shows the corresponding Horizontal-Mura severity level for different ratios of T10, T5, T9, T2 and T7. When T2 and T10's size decrease, Horizontal-Mura phenomenon becomes slight significantly. The reduction of T7 channel number has no obvious effect on phenomena for T7 Size is smaller than T10 and T2; The reduction of T5 and T9 channel number has indirect effect on phenomena, and the effect on phenomenon is less than that of T10 itself.

Tab.1 Severity levels corresponding to T10, T5, T9, T2 and T7 ratios

TFT		T10	T5	T9	T2	T7	Level
Size(μm)		600	150	60	840	240	-
TFT Channel Number		5	6	2	4	2	L5
Numbers Changed by Laser	Case1	4	6	2	4	2	L4
	Case2	3	6	2	4	2	L3
	Case3	2	6	2	4	2	L2
	Case4	5	6	2	4	1	L4
	Case5	5	2	1	4	2	L3
	Case6	5	6	2	2	2	L2
	Case7	5	3	1	2	2	L1
	Case8	2	3	1	3	2	L0
	Case9	2	6	2	2	2	L0

3.3 Leakage Current

As shown in Table 2 the smaller channel length is, the more serious the phenomenon is. The leakage current of TFT is positively correlated with the Width/Length ratio of channel and OL (the overlapping distance between source/drain and gate) [6]. After determining the layout of Mask, the trend of channel length with process fluctuation is just opposite to that of OL.

The 12T1C GOA model in this paper is very dependent on the stability of TFT characteristics. Under the condition of fixed working voltage (VGL and VGH), the drift of TFT transfer curve (up and/or right) will increase the leakage current. Therefore, the 12T1C architecture in this paper cannot be used for products without stable TFT characteristics.

Tab.2 Channel Length and Severity Level

Channel Length	I_{off}	Level
3.5μm	1.5e-10A	L5
4.0μm	3.5e-11A	L0

4 CONCLUSION

GOA has been the mainstream of line addressing design in display, and the excellent display quality much depends on the correct output of GOA. At present, the

major design departments adopt different GOA model. The 12T1C analyzed in this paper is a special one, where the stable high level of voltage Gout's Gate (PU) is the key to ensure that the reset of Gout can follow CLK signal strictly. The stability of PU is easily affected by the ratio of TFT with functions (reset and denoise of PU) and the characteristics of TFT (leakage current) in GOA. This particularity of 12T1C architecture needs the attention of GOA designers. It is innovative to analyze the working state of GOA by laser cutting in GOA region. Referring to the Horizontal-Mura's analysis method in this paper, almost all GOA failure phenomena can be studied.

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