Advanced TFT Modeling Techniques for GOA Driver Circuit Design Optimization

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Key words：TFT compact model, GOA, TFT Modeling Techniques

Abstract

The design methodology for gate driving circuit (GOA) is critical to reduce the production cost and power consumption for TFT-LCD. The process fluctuation in the manufacturing of TFT can cause the malfunction of GOA. TFT compact model is the key to take process fluctuation into consideration during design stage. The testing method and corner modeling for process fluctuation are discussed in this paper. The bin model methodology is also used to help optimize the W/L size of GOA drive circuit. A high reliable A-Si TFT GOA was designed by combining the usage of corner model and bin model.

Introduction

As cell phones and large size TV are becoming more and more popular in our life. TFT-LCD plays the indispensable role of intermediate between 3C product and human beings. LCDs display using a-Si:H TFT technology as backplane is still the major product in large size display field.

GOA technology is integrates the gate drive circuit (Gate Driver IC) on the array (Array) substrate, which has the following advantages: (1) The grid drive circuit is integrated on the array substrate, which can effectively reduce the production cost and power consumption; (2) The GOA technology can save the bonding yield and promote the product yield and productivity; (3)The gate drive circuit gate-IC bonding area is omitted, so that the display panel has a symmetrical structure and can realize the narrow border of the display panel.

However, it exist process fluctuation problem in the manufacture of TFT and GOA driver circuit for TFT-LCD. We should know poor TFT performance which is due to the process fluctuation whether can also satisfy GOA circuit. In addition, it is important to predict the each W/L size TFT properties because that there are many kinds of different W/L size. The main purpose of this work is to find circuit margin by using corner model and predict different W/L TFT size performance using binning model.

2. Results

2.1 Driving of GOA Circuit

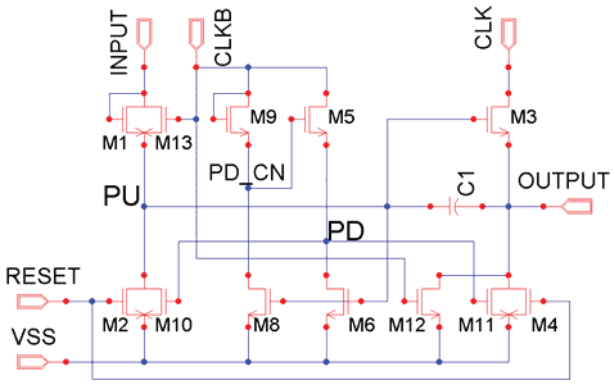

Fig.1 The schematic diagram of proposed GOA driving circuit

Fig.1 shows the schematic diagram of proposed GOA driving circuit. This circuit contains some TFTs with small width over channel length (W/L). As channel length (L) has little impact on device stability, W/L can amplify with same ratio to improve the process uniformity. Duty ratio of GOA clock signal (CLK) could be modified to improve the TFT stability after long time operation and guarantee our GOA circuit performance.

In the GOA driver circuit, TFT Plays important role. TFT performance may change due to fluctuations in the production process should also be reflected in the simulation. The approach is to establish a corner model that includes the device process fluctuation TFT.

2.2 GOA driving circuit using corner model

The Corner Model provides a method and a device for testing a process fluctuation. The process fluctuation testing method includes: obtaining test data of a display substrate to be tested; obtaining a target parameter group from the test data; calculating an average value of each parameter group in the target parameter group. Degree numbers disserting; multiple fluctuation parameter points are calculated according to the average value and the discrete degree number of each parameter group; and the multiple fluctuation parameter points are compared with a plurality of standard parameter points calculated according to the standard parameter group and obtained. Process fluctuation test results.

In the actual TFT manufacturing process for

GOA driver circuit for TFT-LCD, there will be some fluctuations in the process, so that there is a difference between TFT performances of the same size on the same substrate and in different positions. For example, the thickness of the TFT gate insulation at some locations is less than the value set by the process. This will make the capacitive adjustment ability of the TFT enhanced, and the response speed of the TFT is fast. Conversely, the thickness of the TFT gate insulating layer in some places becomes thicker, so that the gate control ability becomes weak and the performance of the TFT deteriorates with respect to the process setting value. This change in the TFT performance due to fluctuations in the production process should also be reflected in the simulation. The approach is to establish a corner model that includes the device process fluctuation TFT, it is determined which targets to focus on and the offset of each target with respect to the normal value, then the adjustment of the related parameters makes each device target become the offset value of the corner model. What needs to be clear is whether to increase or decrease in each target.

In this paper, the corner model is based on the established TFT model which is only focuses on target when it is created. As is shown is Fig.3a, first, we have measured the TFT electrical characteristics (Vth, Ion, Isat, Ioff) through TEG (Key sight 5270B) of 9 positions on the G8.6 large-size TFT-LCDs. Choosing the GOA driver circuit which TFT size will used, like W100, W500, W1000, W5000 TFT size for measuring to architecture GOA circuit on other sizes.

Then, distributing statistics on performance data obtained in step one. For T4 (W1000) as an example, we graphically displayed physical combination shown in Fig.3b-f, Ion-Vth, Isat-Vth, Ion-Ioff, Ion-Isat, and Ioff-Isat. Third, creating a target form by the analysis of data showing in Fig.4.

Moreover, we have adjusted the difference IDVG curves in model which is shown in Fig.5a. As is shown in Fig.5b is the TT Target fitting results in model.

In the Fig.6, we have put the results of the model fitting into the spice to obtain the TT, FF, SS curve. The simulation results will have a feedback effect on the process and it is necessary to verify that the product is working as expected.

As is shown in Fig.7, the difference between the simulated value and the model value is within a small error range.

In the Fig.8, it is the schematic of the GOA output waveform. The figure shows the parameters closely related to the drive: Vmax, Tr, and Tf. Vmax represents the highest potential of the output waveform, the higher the potential, the stronger the driving ability. Tr and Tf represent the rise time of the waveform at 10%~90% and the fall time of 90%~10%, respectively, where Tf is the most important GOA output parameter that needs attention in design and Tf is as small as possible. In our GOA design results, FF Vmax (29.26V) larger than SS (28.54V) and Tf (4.93us) is shorter than SS (7.05us). It turns out to be that the SS also can pass the GOA driver circuit.

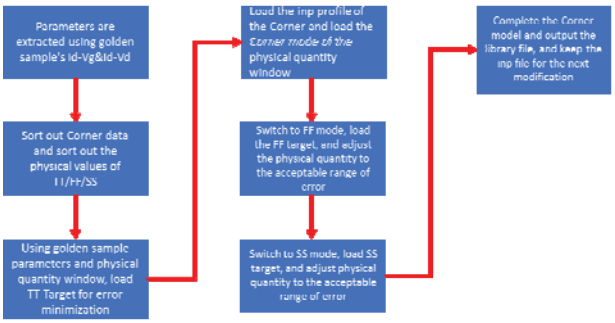

Fig.2 Diagram of corner model extraction flow

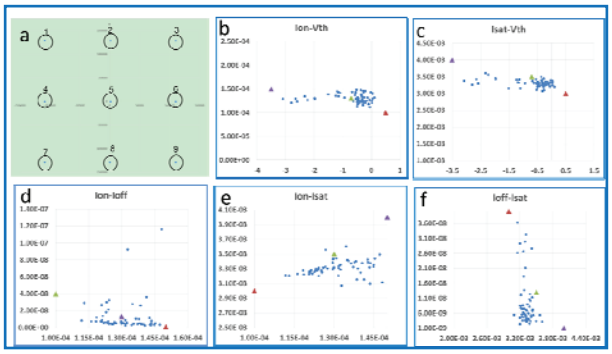

Fig.3 Analysis of measured data

	Vth(V)	Ion(A)	Isat(A)	Ioff(A)
SS	2.5	1.10E-05	1.10E-04	4.00E-09
TT	-0.3	1.35E-05	1.30E-04	9.00E-10
FF	-2	1.55E-05	1.60E-04	3.00E-10

Fig.4 Creating typical (TT), fast (FF), and slow (SS) target according to analysis results

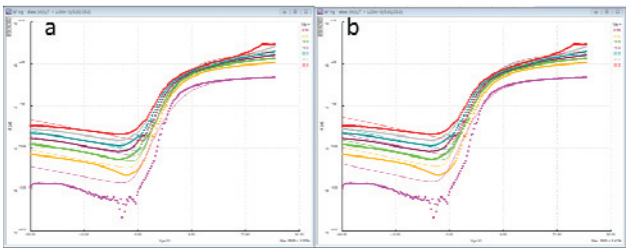

Fig.5 (a) The best I-V fitting by Model and (b) TT Fitting Results by Model

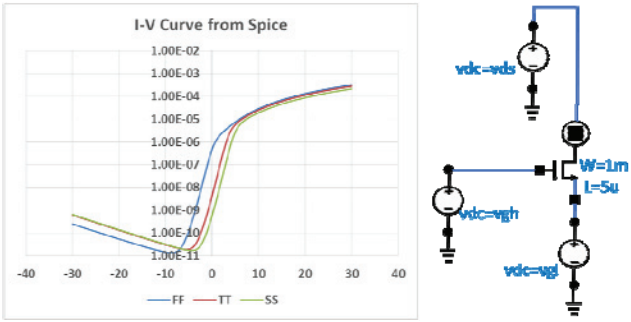

Fig.6 Spice Results of FF&TT&SS （Left is FF, Middle is TT, Right is SS ）

	VD=0.5	VD=5	VD=10	VD=15	VD=20	VD=25	VD=30
TT error %	0.0036%	0.0036%	0.0036%	0.0035%	0.0035%	0.0034%	0.0033%
FF error %	0.0036%	0.0036%	0.0036%	0.0035%	0.0035%	0.0035%	0.0034%
SS error %	0.0036%	0.0036%	0.0036%	0.0036%	0.0035%	0.0034%	0.0034%

Fig.7 The comparison chart for the outcomes of TFT Protractor ELDO

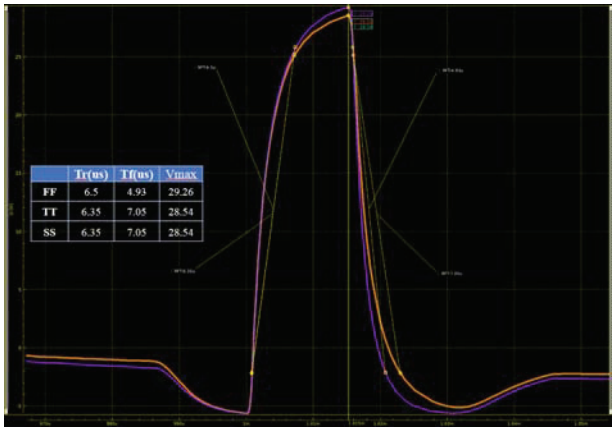

Fig.8 The schematic of the GOA output waveform of ff, tt and ss

2.3 GOA driving circuit using binning model

In the GOA driver circuit, it is important to predict the each W/L size TFT properties because that there are many kinds of different W/L size. The W size TFT from tens to tens of thousands, but large-size TFTs have TFT burnout during measurement, so it is necessary to predict the performance of other W size TFTs from existing data. The approach is to establish a Binning model that can predict different W/L TFT size performance

The Binning model is to establish a point model for each TFT in a set of data, corresponding to a model card and a set of model parameters, then mathematically combine all the point models into a model that can cover this size range. Schematic diagram of test data distribution in Binning model, with this feature, a set of specific model parameters can be adjusted for different values of drawn channel length and width to provide a better current characteristic of device when doing the circuit simulation.

Fig.9 shows the Schematic diagram of test data distribution in Binning model and Fig.10 shows the new added on binning parameters for original Level 61 parameters. In Fig.11, it is the binning model making, after the different W size (W100, W500, W1000, W5000) TFT accomplished the model card fitting, binning model can be made. Last but not least, we have checked the binning model by using a working principle of a circuit of a TFT in Fig.12. The result shows bigger the W size, the bigger Ion, after checking the Binning results is right, Bring binning to the GOA circuit. Finally, 43 FHD LCD driven by GOA was successfully demonstrated.

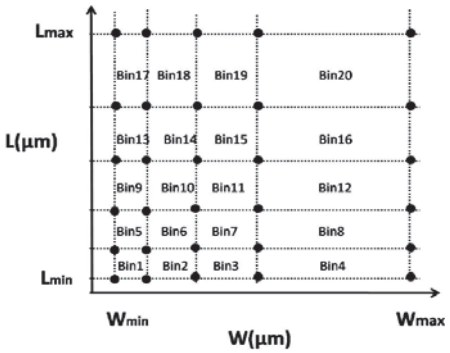

Fig.9 Schematic diagram of test data distribution in Binning model

$$P = VTO + \frac{LVTO}{L} + \frac{WVTO}{W} + \frac{PVTO}{L*W} \quad (1)$$

For each size of device, a point model is used to integrate the point model by introducing L, W, P related parameters. The accuracy of the model is high.

$$P1 = VTO + \frac{LVTO}{L1} + \frac{WVTO}{W1} + \frac{PVTO}{L1*W1}$$

$$P2 = VTO + \frac{LVTO}{L2} + \frac{WVTO}{W2} + \frac{PVTO}{L2*W2}$$

$$P3 = VTO + \frac{LVTO}{L3} + \frac{WVTO}{W3} + \frac{PVTO}{L3*W3}$$

$$P4 = VTO + \frac{LVTO}{L4} + \frac{WVTO}{W4} + \frac{PVTO}{L4*W4} \quad (2)$$

Parameter	L Term	W Term	P Term	Notice
ALPHASAT	LALPHASAT	WALPHASAT	PALPHASAT	
CGDO	LCGDO	WCGDO	PCGDO	
CGSO	LCGSO	WCGSO	PCGSO	
DEF0	LDEF0	WDEF0	PDEF0	
DELTA	LDELTA	WDELTA	PDELTA	
EL	LEL	WEL	PEL	
EMU	LEMU	WEMU	PEMU	
EPS				
EPSI				
GAMMA	LGAMMA	WGAMMA	PGAMMA	
GMIN	LGMIN	WGMIN	PGMIN	
IOL	LIOL	WIOL	PIOL	
KASAT	LKASAT	WKASAT	PKASAT	
KVT	LKVT	WKVT	PKVT	
LAMBDA	LLAMBDA	WLAMBDA	PLAMBDA	
M	LM	WM	PM	
MUBAND	LMUBAND	WMUBAND	PMUBAND	
RD	LRD	WRD	PRD	
RS	LRS	WRS	PRS	
RDX	LRDX	WRDX	PRDX	
RSX	LRSX	WRSX	PRSX	
RDSMOD				
SIGMA0	LSIGMA0	WSIGMA0	PSIGMA0	
TNOM				
TOX				
V0	LV0	WV0	PV0	
VAA	LVAA	WVAA	PVAA	
VDSL	LVDSL	WVDSL	PVDSL	
VFB	LVFB	WVFB	PVFB	
VGSL	LVGSL	WVGSL	PVGSL	
VMIN	LVMIN	WVMIN	PVMIN	
VTO	LVTO	WVTO	PVTO	

Fig.10 The new added on binning parameters for original Level 61 parameters

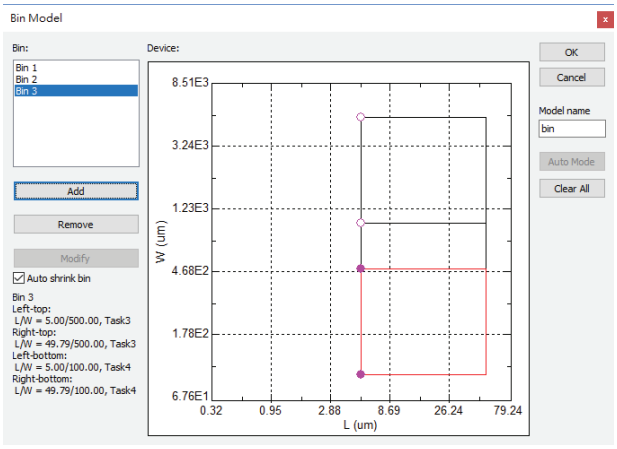

Fig.11 The binning model making

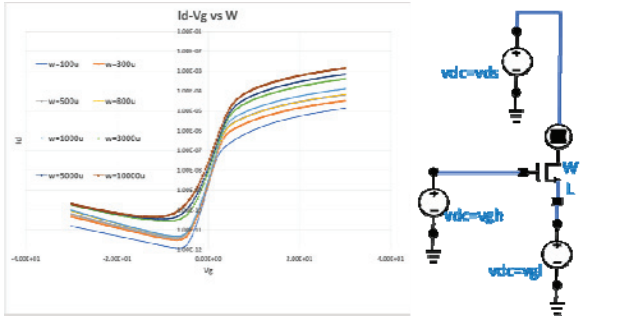

Fig.12 Spice Results of Binning model with different W size for GOA

2.4 Light-on images for 43” FHD using GOA driving circuit

The photograph of display image is shown in Fig.13.

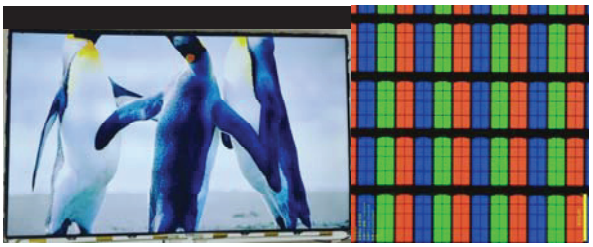

Fig. 13 Light-on images for 43” FHD using GOA technology

2.5 Life Time

Model has a set of innovated proprietary stress and hysteresis model and smart engine to help users to estimate the TFT device lifetime under given stress condition. With the single push-button feature, the Model can quickly calculate the TFT device lifetime with the pre-installed compact equations and provides the reliability prediction. We have checked our TFT lifetime, the stress VDS 1V and VGS 20V,Stress temperature 70℃， T0 Vth is -0.2V and the target Vth is 4V， we get the lifetime 5750s which demonstrate that the TFT has good properties.

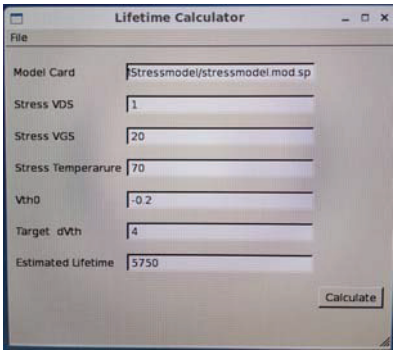

Fig. 14 Life time of 43” FHD using GOA driving circuit results

3. Conclusions

A GOA circuit driver was used in the manufacture of TFT-LCD and the LCD Panels were lighten on. The Process fluctuations in the manufacture of TFT and GOA drive circuit for TFT-LCD have been checked by corner model. The Binning simulation and spice was used for easily predict the W/L size for GOA driver circuit so that we can save the manufacturing time and avoid large-size TFTs burnout during measurement.

Acknowledgement

This work was supported by HKC optoelectronics technology, China.

References

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