A Narrow Border Design and Low Power Consumption of a-Si:H TFT Gate Driver Circuit

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Abstract

In this paper, an integrated hydrogenated amorphous silicon (a-Si:H) thin-film transistor (TFT) gate driver circuit design for narrow border and low power consumption in the small-size panel is proposed. The border can be decreased from 1 mm to 0.8 mm, which can be further improved to 0.65 mm. In addition, the power consumption of circuit can be reduced by using the 25% duty ratio 8 clock signals with high reliability.

Author Keywords

Gate driver on array; GOA; Narrow border; Low power consumption;

1. Introduction

In recent years, the demand of high screen ratio for the display is become more and more popular in the market. In order to increasing the screen ratio, the border of cell should be as narrow as possible [1-3]. The hydrogenated amorphous silicon thin film transistor (a-Si:H TFT) for the gate driver on array (GOA) circuit has been widely used in the flat panel display for several years. However, the mobility of a-Si:H TFT is about 0.2~0.4 cm^2/V-s, which is less than that of oxide and low temperature poly silicon. It indicated that the size of the a-Si:H TFT should be much large to drive the gate line loading. Therefore, the number of TFT in the GOA unit is need to be control at the minimal value and the parameters should be optimized for the narrow border. In addition, the low power consumption of portable electronics is necessary for the long time operation. The power consumption of GOA is related to the voltage, frequency and parasitic capacitance of signal lines.

In this paper, we proposed a new GOA circuit design which can decrease the border from 1 mm to 0.8 mm without affecting the reliability. The narrow border design is to simplify the connection line between the stage, which can save more space to achieve narrow border. Furthermore, it can be reduced to 0.65 mm by combining the capacitor into the TFT via three metal design and gate insulator contact hole. The 25% duty ratio 8 clock signals are adopted in the circuit to reduce the power consumption. As a consequence, the stable and low power consumption with narrow border GOA circuit are presented.

2. Proposed Integrated Gate Driver Circuit

Figure 1(a) shows the new GOA circuit and the block diagram of the stage. The signal line connection of stages for the panel is shown in fig. 1(b). The timing diagram of 25% duty ratio 8 clock signals are shown in fig. 1(c). The power consumption of circuit can be estimated by the following formula [4]

$$\text{Power} = V_{DD} * I_{avg} = V_{DD} * [C * V_{Swing} * Fck]/2$$

, where V_{DD}, I_{ave}, C, V_{Swing}, F_{ck} are the supply voltage, average current from the supply, loading capacitance, average swing voltage of clock, and the clock frequency. From the formula, the power consumption of new GOA circuit can reduce about 30% power consumption due to the lower frequency and the lower capacitance of clock signals.

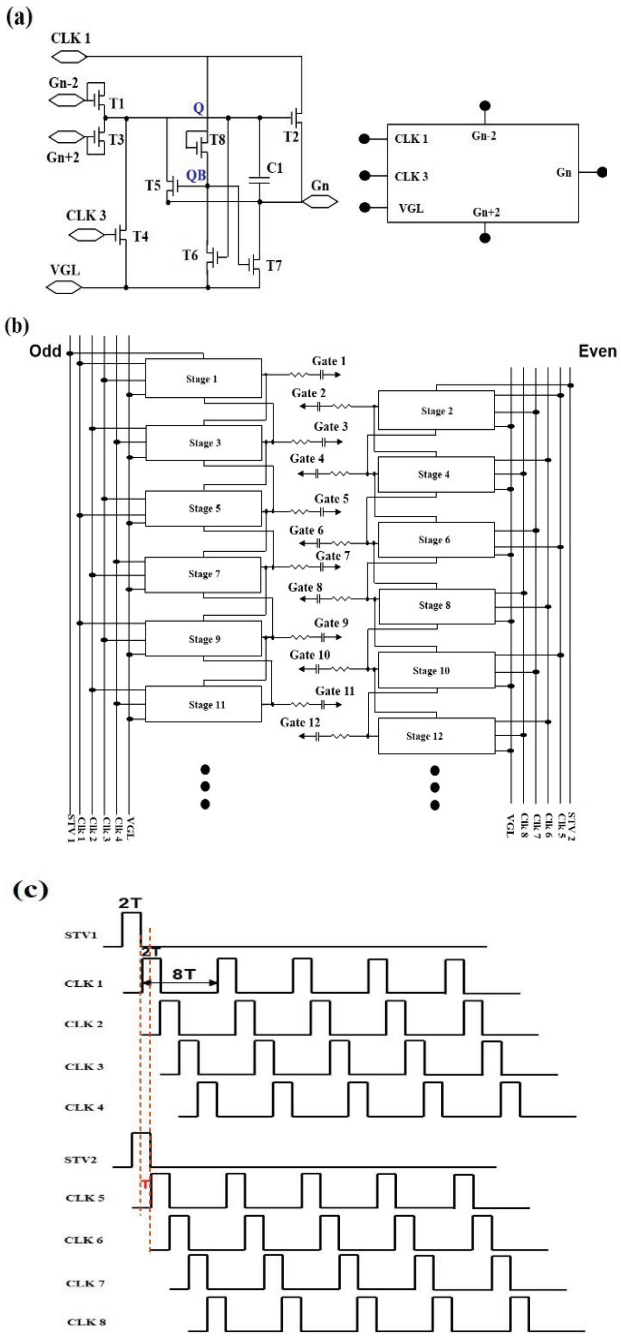


Figure 1. (a) The structure of new GOA circuit and the block diagram of the stage. (b) The connections between

stages of the proposed circuit for the in-cell touch panel. (c) The timing diagram of signals.

Figure 2 shows the timing diagram of signals and the output waveform of gate 1. In the period 1, the T1 is turned on by the STV 1 and then pre-charge the Q node, leading to that the T6 is turned on to discharge the QB node to the VGL and then the T5 and T7 are turned off. In the period 2, the CLK1 is from the low voltage level to the high voltage level and then the gate 1 is charged by T2. At the same time, the Q node is boosted through C1 to the higher voltage increases the output ability. It is worth to mentioned that the size of T6 is much large than T8 to ensure that the QB node can be maintained at the VGL. In the period 3, the CLK 2 is at the low voltage level to discharge the gate 1 by T2, and the Q node is coupled via C1 to the lower voltage. In the period 4, the Q node is completely turned off by the T4 turned on from the CLK3 then turn off the T6. In the period 5, the QB is charged through the T8 periodically, turning on the T5 and T7 to maintain the Q node and gate 1 at the VGL, respectively. As a result, the waveforms of gate 1 is generated by the gate driver circuit successively.

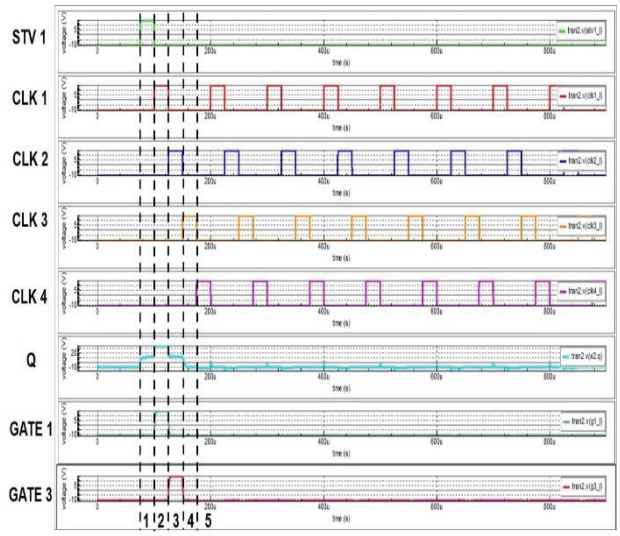


Figure 2. The timing diagram of signals and the output waveform of gate 1.

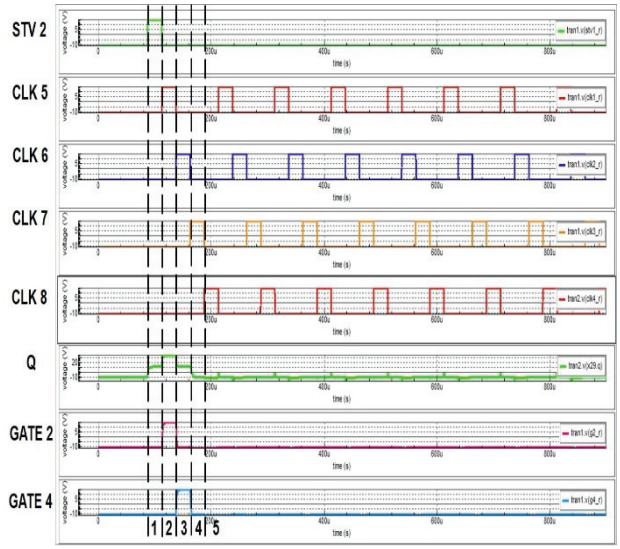


Figure 3. The timing diagram of signals and the output waveform of gate 2.

3. Simulation Results

Figure 3 shows the timing diagram of signals and the output waveform of gate 2. The output mechanism of even and odd part is the same. The signals of STV 2, CLK 5~8 are delay a horizontal time compared to STV1, CLK 1~4, respectively. Figure 4(a) shows the simulation output waveforms from the first to final gate at the 27°C. Each gate overlaps one horizontal time with another gate, indicating that the pre-charge time is one horizontal time, as shown in fig. 4(b). Figure 4(c) shows the simulation of output waveforms at the 70°C and the threshold voltage (V_{th}) shift 3V. It can be seen that the noise of waveforms at the 70°C become higher, but it still be controlled below the -10 V, which ensures that the circuit can normally operate.

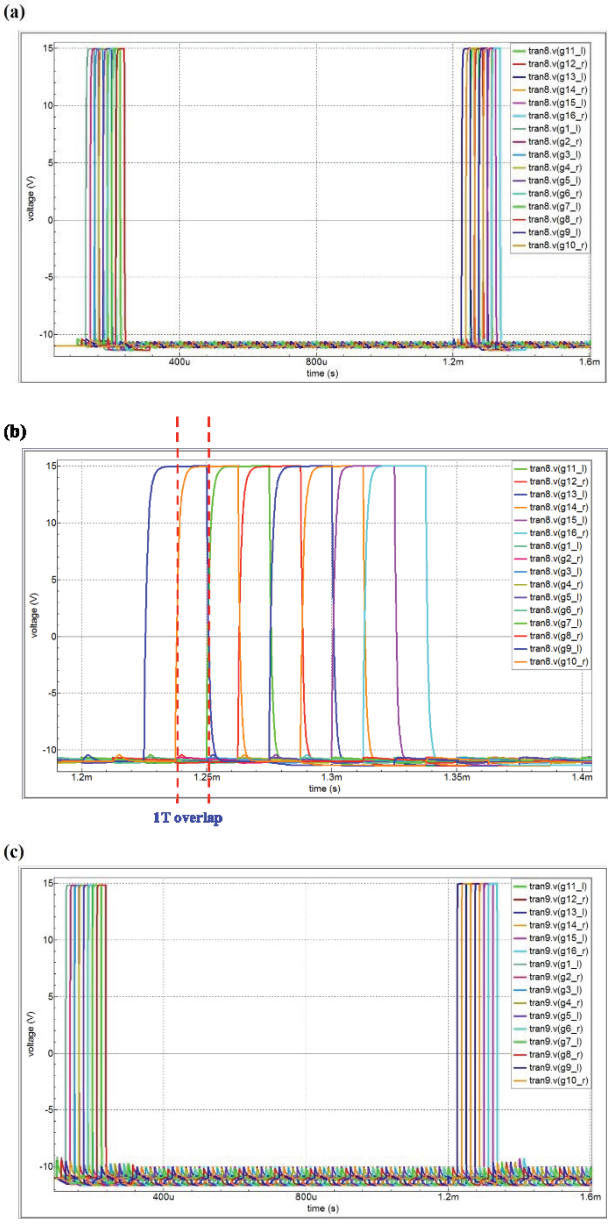


Figure 4. (a)The simulation output waveforms of gate at 27˚C. (b) The last 8 output waveforms of gates. (c) The simulation output waveforms of gate at 70˚C (V_{th} shift 3V).

4. Narrow Border design

Figure 5 (a) shows the layout of proposed GOA circuit. Each stage has a 180 μm height and 0.8 mm width including the clock routing area. There is an 80 μm space on the right side for the cutting process accuracy, and the 100 μm space of left side is for the common electrode connection. Figure 5 (b) shows the image of fabricated GOA circuit. The narrow border of 0.8 mm can be achieved is attributed to the simple connection. The output waveform of stage is transmitted to the T1 of next stage and to the T3 of previous stage (red line in the fig. 5(b)), and the function of T3 in the circuit is only for the bi-direction scan. Thus, the border can be further reduced to 0.65 mm by removing the T3, combing the T2 and C1 via three metal design, and adding additional mask of gate insulator contact hole, as shown in figure 6. Figure 7 shows the simulation of proposed GOA circuit removing T3, which is the same with the previous output waveforms.

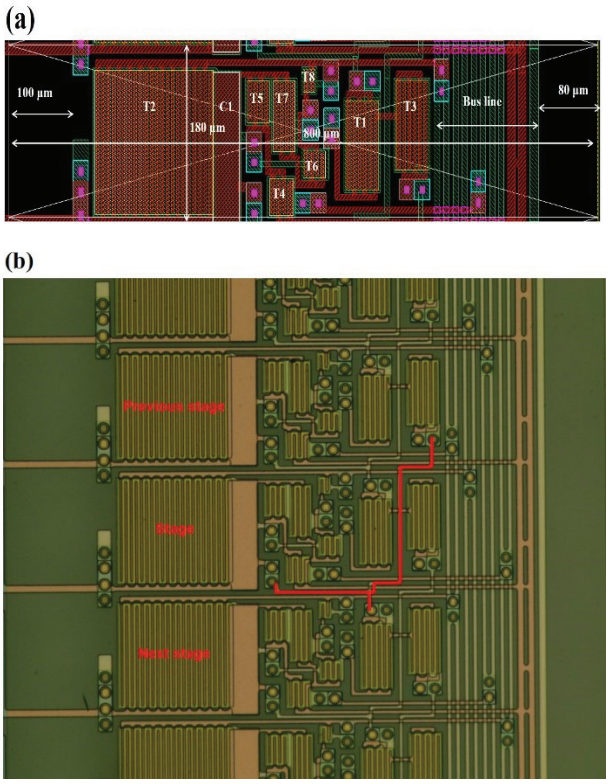


Figure 5. (a) The layout of proposed GOA circuit. (b) The image of fabricated GOA circuit.

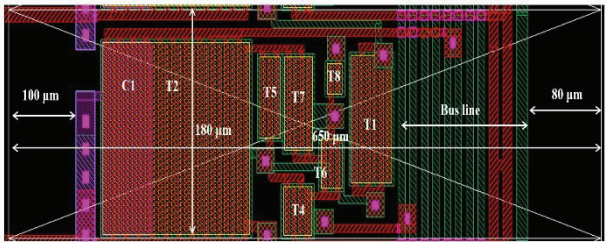


Figure 6. The layout of proposed GOA (0.65 mm).

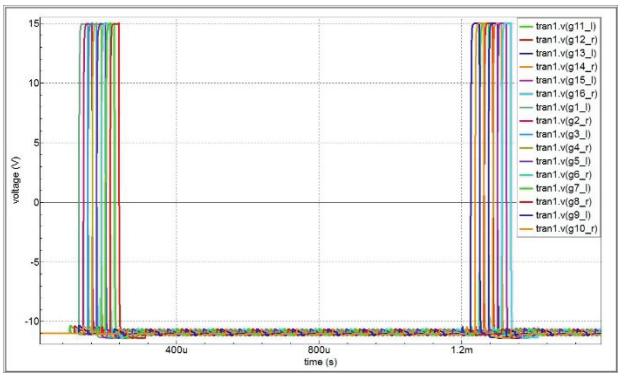
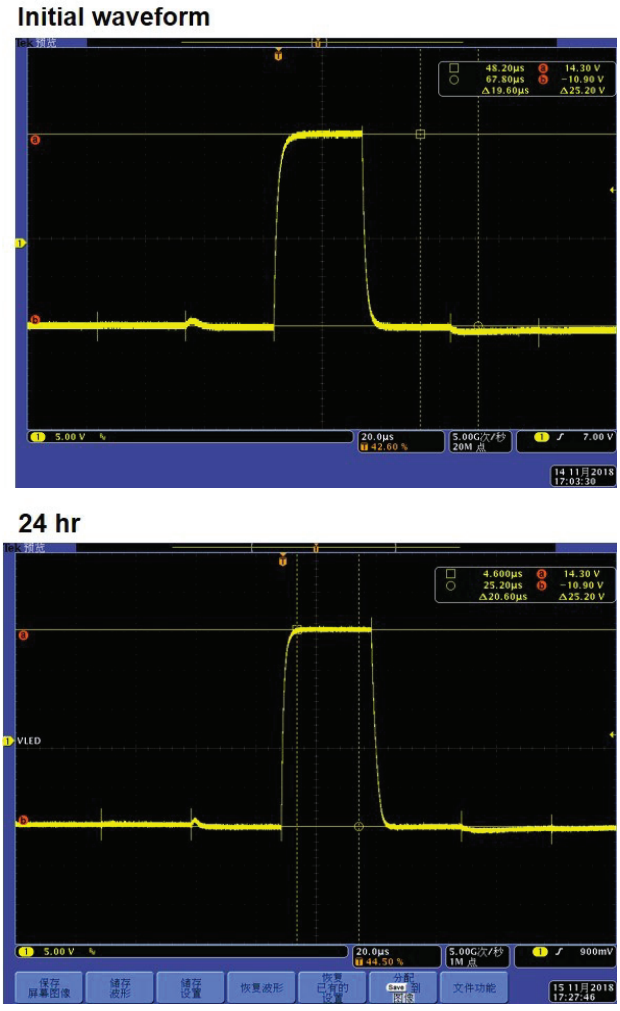


Figure 7. The simulation of proposed GOA circuit removing T3.

5. Reliability test

Figure 8 shows the reliability test of GOA circuit at 70˚C for a long time operation, and the output waveform is the final stage. It can be seen that the waveform is almost the same after the 120 hr reliability test, indicating that the circuit still can work after long time high temperature operation.



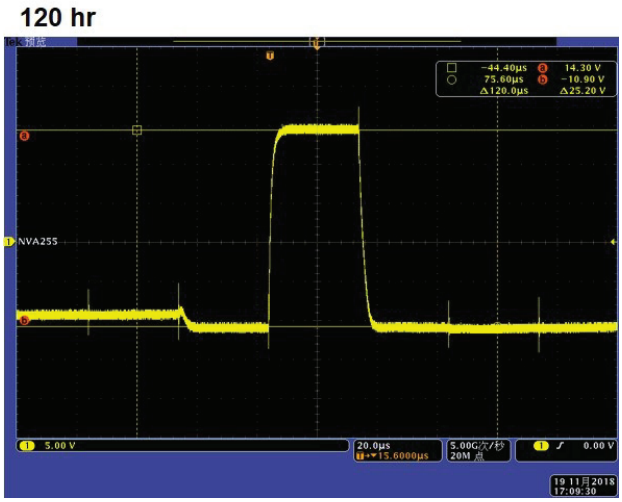


Figure 8. The output waveform of final stage in 70˚C at different operation time.

6. Conclusions

In summary, we have demonstrated the new GOA circuit with narrow border, low power consumption and high reliability. The narrow border with 0.8 mm is fabricated by using a simple connection between the stages, which can further decrease to 0.65 mm. The 25% duty ratio 8 clocks are adopted to the circuit, resulting in the low power consumption. The reliability test show that the circuit is stable after a long time high temperature operation.

7. References

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