Comparing Single Gate TFT to Dual Gate TFT for OLED Compensation Circuit

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ABSTRACT

Dual gate TFT has been widely used for AMOLED pixel compensation circuit to reduce leakage current and to have good reliability. The study shows that single gate TFT has better off-state performance than dual gate TFT. Therefore, new pixel compensation circuit designed with only single gate TFTs is suggested.

1 INTRODUCTION

The threshold voltage (Vth) canceling circuit has been widely used for OLED pixel compensation circuit, which has diode-connection.[1] The dual gate TFT would be used for diode-connection in order to reduce leakage current and to improve reliability.[2]

However, it is well known that the P-type LTPS TFT is more stable than N-type LTPS TFT under high bias condition. As well, the leakage current cannot be reduced dramatically even with dual gate TFT. So, most of company would use bias-stressed LDD (Lightly Doped Drain) process, so called “TFT aging”, to reduce the leakage current.[3] Fig.1 shows the transfer characteristics of single and dual gate TFT. As we discussed, dual gate TFT without LDD has high leakage current. The LDD in Fig.1 was been formed by bias-stress.

The study is to investigate the actual effect and problems of the dual gate TFT.

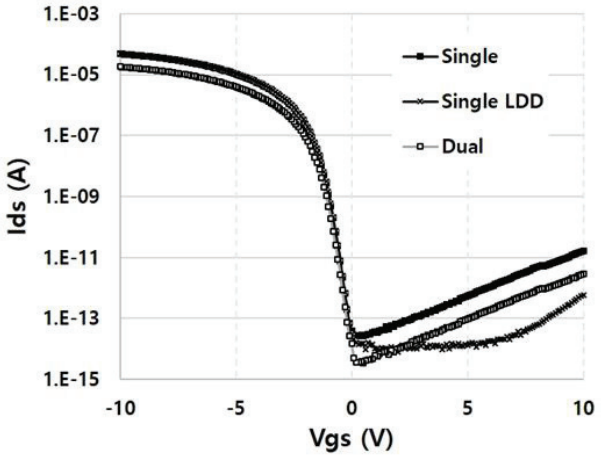


Fig. 1 Transfer characteristics

2 EXPERIMENT

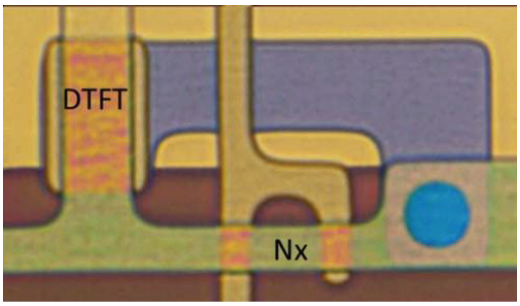
2.1 Coupling effect of floating node

To cancel the Vth, the driving TFT’s gate and drain should be connected. It is called as “diode-connection”.

When the switching signal to operate dual gate TFT is turned off, the charges accumulated in the dual gate are injected to source, drain direction and floating node, Nx as shown in Fig.2. The Nx is affected by twice charges in comparison to source and drain. So, the peak coupling voltage is higher than the voltage of source and drain. In very short time, the high peak voltage at Nx can make leakage current to alter the gate voltage of driving TFT. Generally Nx can be acted as drain of right-side-TFT (RTFT).

However, Nx node can be a source node of RTFT because the voltage of Nx is higher than Vg. As shown in Fig.3, the simulation result shows that the voltage of Nx would be higher than 8V. As well, RTFT would hardly have bias-stressed LDD due to dual gate structure. It means that the leakage current may be higher than our expectation. The voltage variation caused by the small leakage current can affect the brightness on OLED emission.

To reduce the coupling voltage at Nx, we can add capacitive load at Nx. It would reduce the peak voltage. However, the phenomena that Nx acting as source of RTFT cannot be avoided. As well, biasing is also very difficult due to dual gate TFT.



(a)

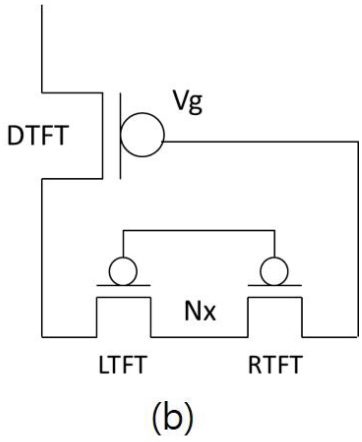


Fig. 2 Diode-connection (a) micro scope image, (b) equivalent circuit

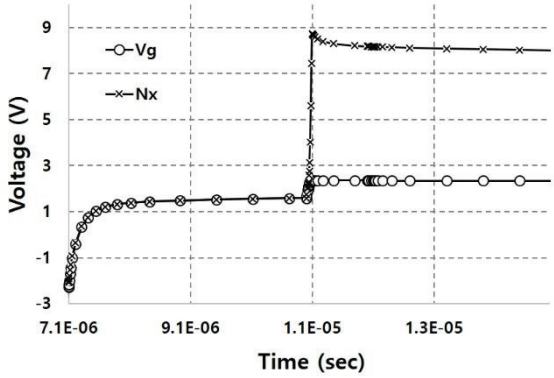


Fig. 3 Voltage of Nx after SPICE simulation

2.2 Bias-stressed LDD

The previous report indicated that P-type LTPS TFT can be easily formed pseudo LDD by bias-stress. Hot electrons would be trapped into gate insulator interface. The captured electrons accumulate holes, it can work as LDD. This phenomenon would more easily occurs as higher electric field. As we know, the purpose of dual gate TFT is to reduce electric field of drain region without LDD. It means that much higher field would be needed to make Bias-stressed LDD in case of dual gate TFT.

Fig.4 shows I-V transfer characteristics of single gate TFT under various bias stress. The data shows that the single gate TFT shows LDD behavior on very short stress time. Table.1 is the comparison dual gate TFT to single gate TFT under various Vds and difference stress time. Single gate TFT shows LDD characteristics on short time and lower Vds. The actual Vds field of dual gate TFT is lower than that of single gate TFT due to field relaxation.

The reliability of single gate TFT has also been evaluated as shown in Fig.5. The reliability of single gate TFT is stable after forming bias-stressed LDD. The performance was not degraded, contrarily, the effective mobility is slightly increased caused by channel shortening. The channel shortening effect is shown to be larger as shorter channel length, however, normalized channel shortening is only time-dependent. Channel shortening length of L = 5μm TFT can be expected to be less than 0.5μm after 1Msec stressing.

The Vth variation has been investigated, the changing was negligible as shown in Fig.4, less than 0.1V after 1ksec hot carrier stressing. NBI (Negative Bias Injection) and PBI (Positive Bias Injection) are important parameters to define reliability, but independent of drain field, those are controlled by gate insulator quality. The evaluating data indicates that reliability of single gate TFT is affordably stable.

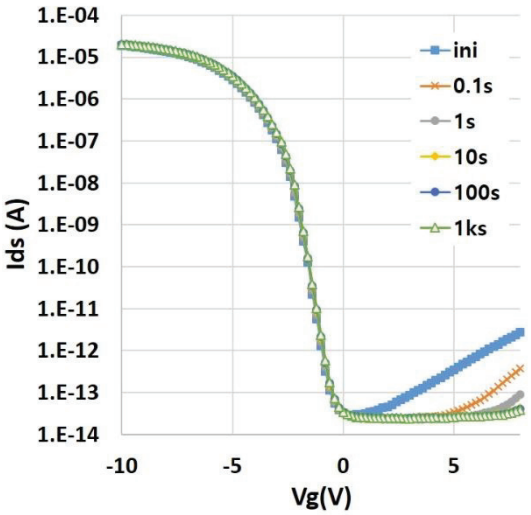
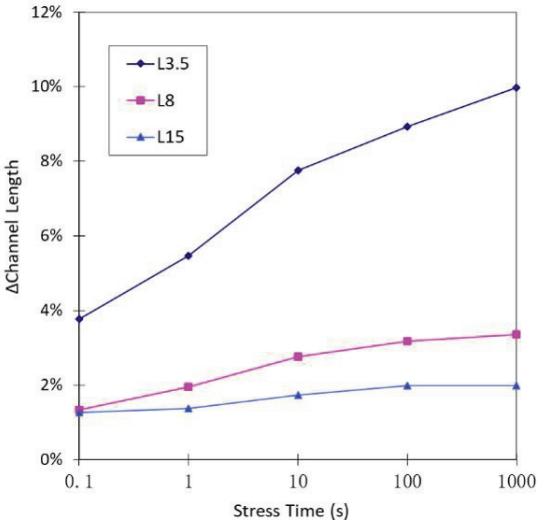


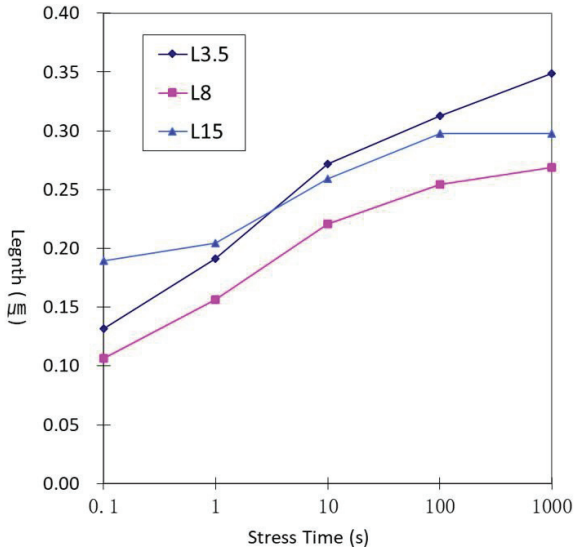
Fig. 4 Single gate TFT characteristics

Table 1 LDD Forming time (@ Vgs = 5V, Ioff < 2pA)

Vds	-5V	-10V	-15V
Single Gate	10s	1s	1s
Dual Gate	30s	20s	5s



(a) Channel length variation ratio



(b) Normalized channel length variation

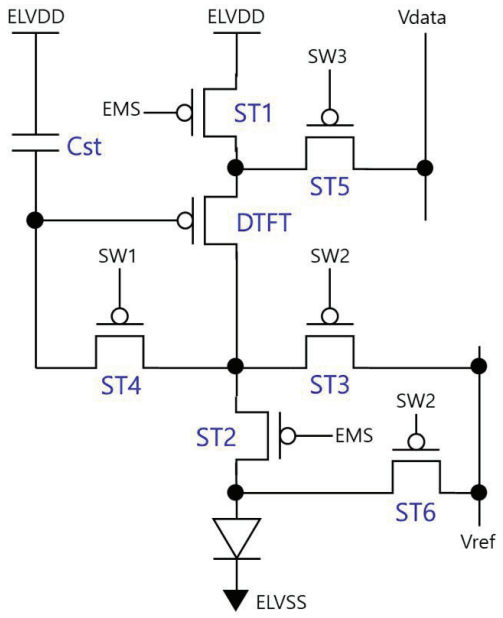
Fig. 5 Mobility variation under hot carrier stress

3 RESULTS

We suggest new compensation circuit as shown in Fig.6. The circuit is a typical Vth canceling circuit based on diode-connection. But, dual gate TFT is not contained to reduce leakage current.

Now, we are evaluating the actual performance of the circuit, focusing on long term reliability. However, our previous study shows that single gate TFT would be effective and stable by using bias-stressed LDD.

The circuit has additional two advantages; one is to save design area due to only using single gate TFT, and the other is that the storage capacitance (Cst) has only one leakage current path. As a result, the new circuit is effective to minimize leakage current and its path.



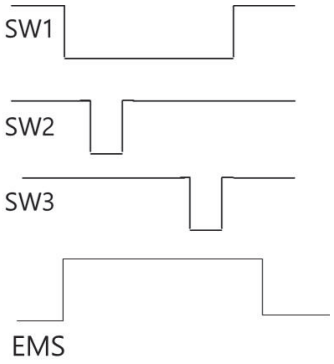


Fig. 6 New compensation circuit

4 CONCLUSIONS

This study indicate that the single TFT for diode-connection is more effective rather than dual gate TFT. Single gate TFT is little affected by coupling and the bias-stressed LDD is more easily formed in single gate TFT. And the suggested new compensation circuit have two advantages; one is to save design area due to only using single gate TFTs, and the other is that the storage capacitance (Cst) has only one leakage current path. As a result, the new circuit is effective to minimize leakage current and its path.

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