

# Factor Analysis and Evaluation Method for Power Degradation of LTPS LCD

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Keywords: Integrated circuit, high PPI, high frequency, high brightness, power consumption

## ABSTRACT

The IC industry has been developing rapidly, and people are becoming more and more interested in the research of IC performance and power consumption. With the increasing demand for mobile communication devices such as mobile phones and tablets, the performance of LCD screens with high PPI, high frequency and high brightness will compete with OLED screens in the market. Based on the current development and application of high frequency 90Hz and 120Hz game phones, all of which severely test designers' thinking about the power consumption of integrated circuits, it can be seen that both consumers and designers have launched a new wave of challenges to the battery life of integrated circuits.

## 1 INTRODUCTION

For a long time, the most important problem in the design of high speed digital integrated circuits is to reduce the power consumption. Due to the waste heat generated by energy consumption, the circuit components are affected to different degrees. When the temperature reaches a certain level, the circuit will not work normally, and the performance of the whole machine is bound to be reduced. In addition to the demand and development of quick response of high frequency products such as 90Hz and 120Hz, the power consumption of panel doubles compared with that of 60Hz. The Figure 1 is the comparison of product power consumption measured at different frequencies.

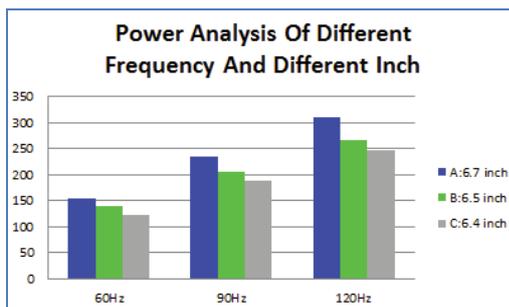


Figure 1. Power Analysis Of Different Frequency And Different Inch

For electronic products with long life cycle and high reliability, the fast loss of power consumption is bound to affect customer experience. Therefore, reducing power consumption is an inevitable trend.

This paper makes the following research on reducing the power consumption of IC: (1) general IC power analysis and calculation method interpretation; (2) cell phone panel power consumption disassembly reading; (3) establish power consumption simulation mechanism for important factors after disassembly; (4) through the optimization and improvement of the above content to find

the design method and design skills to reduce power consumption.

By comparing the experimental data, the author summarizes the feasibility measures of designers to reduce the power consumption of integrated circuits. Therefore, it is of great significance to study the circuit design technology to reduce power consumption.

## 2 THEME

### 2.1 Power analysis and calculation method of integrated circuit

Integrated circuit power includes two parts: dynamic power and static power<sup>①</sup>.

The consumption generated when the device turns on the current is called dynamic power consumption. In other words, the loss of energy due to the change of signal waveform inside the circuit, including the switching power consumption caused by the capacitor charge and discharge and the short-circuit power consumption caused by the through-current.

When all device signal waveforms are constant, the power loss caused by circuit leakage is called static power loss. Nowadays, with the improvement of the resolution of the panel and the compression of the frame, the channel limit of MOS devices is constantly challenged, which makes the power consumption increase exponentially. The proportion of static power consumption in total power consumption can not be ignored.

$$P_{total} = P_{switch} + P_{short} + P_{leak}$$

switching power consumption is:

$$P_{switch} = f C V_{dd}^2$$

C: load capacitance;

f: clock frequency;

$V_{dd}$ : supply voltage

(Equation 1)

It can be seen that the capacitance of the circuit, the clock frequency, the square of the voltage is proportional to the relationship, so can reduce from the above several aspects.

Short circuit power consumption

$$P_{short} = \frac{\int_0^t T dt}{T} V_{dd} = \frac{\int_0^t I dt}{T} (V_{dd} - V_{th})$$

$\frac{\int_0^t Idt}{T}$  : the average current of the electrical frequency signal up or down until the specified time;

$V_{dd}$  :The power supply voltage;

$V_{th}$  :The threshold voltage)

(Equation 2)

Therefore, switching power consumption can be reduced by lowering the device threshold voltage and reducing the delay time of short electrical frequency signal line.

For conventional MOS circuit, there is no dc conduction current when it is stable, so the static power consumption is 0 in the ideal state. However, due to the existence of device leakage, the static power consumption of the circuit is subject to the effect of parasitic PN junction current and MOS tube subthreshold leakage current to generate additional current. Thus it can be seen

Static power:

$$P_{leak} = I_{leak} V_{dd}$$

$I_{leak}$  :Leakage current;

$V_{th}$  :The threshold voltage

(Equation 3)

Therefore, to reduce the static power consumption of integrated circuits, we should not only improve the process capacity to reduce the leakage degree of devices, but also consider the renovation of circuit design. We will continue to dissect panel power consumption in the next text.

## 2.2 Dismantling method of panel power consumption

The power consumption of MOD is about 80% due to backlight consumption, and the remaining 20% comes from the energy loss on the CFOG side. This paper mainly analyzes the important factors affecting the 20% power loss. This is shown below. The structure of the Panel includes DEMUX, VSR, AA, Fanout and other components which is shown on Figure 2. And each part has a different proportion of power consumption in operation. This paper will disassemble each proportion.

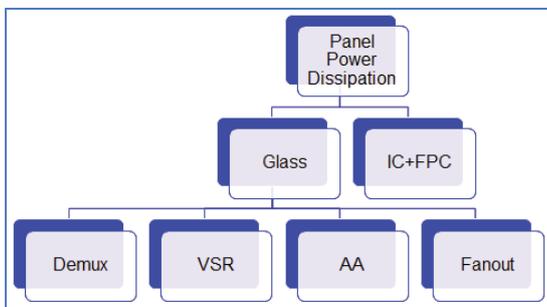


Fig.2 The Structure Of Panel Power Consumption

Therefore, the decomposition formula of panel power consumption is as follows:

$$P_{panel} = P_{demux} + P_{VSR} + P_{AA} + P_{IC+FPC} + P_{Fanout} \quad (\text{Equation 4})$$

For consumer products, we use three groups of voltage values: the input voltage IO of the fixture, the input voltage VGH of the Panel, and the input voltage VGL of the Panel. Through experimental measurement of working voltage and working current under different detection screen and the method of addition, subtraction, multiplication and division, the author makes fast calculation, which is simple and clear to realize the dismantling of the theoretical basis of digital circuit, so that readers can fully understand.

Measure the voltage and current value of a 60Hz panel under 5 kinds of measuring screen: R screen, black screen, white screen, 1\*1Bar (G128), Pixel check (G128).

Take the white screen for example:

$$P_{normal} = V_{IO} * I_{IO} + V_{VGH} * I_{VGH} + V_{VGL} * I_{VGL} = 120.7mW$$

$$P_{CKV\text{关闭}} = V_{IO} * I_{CKV\text{关闭}} + V_{VGH} * I_{CKV\text{关闭}} + V_{VGL} * I_{CKV\text{关闭}} = 116mW$$

$$P_{CKV\&CKH\text{关闭}} = V_{IO} * I_{CKV\&CKH\text{关闭}} + V_{VGH} * I_{CKV\&CKH\text{关闭}} + V_{VGL} * I_{CKV\&CKH\text{关闭}} = 96.6mW$$

$$P_{CKV} = P_{normal} - P_{CKV\text{关闭}} = 120.7 - 116 = 4.7mW$$

$$P_{CKH+AA} = P_{normal} - P_{CKH\text{关闭}} = 120.7 - 103.1 = 17.6mW$$

$$P_{CKH+CKV+AA} = P_{normal} - P_{CKH\&CKV\text{关闭}} = 120.7 - 96.6 = 24.1mW$$

(Equation 5)

By this method, the power consumption values of each part can be calculated under the following 5 detection images: R screen /black screen /white screen /1\*1Bar (G128) /Pixel check (G128). The results is shown on Figure 3. Thus, the proportion of each part can be obtained. From the power dismantling, we know that the power loss caused by CKV is the largest except IC and FPC, so what causes the large impact of CKV? (PS: excluding data errors caused by short-circuit and other influencing factors caused by device shutdown in the experiment).

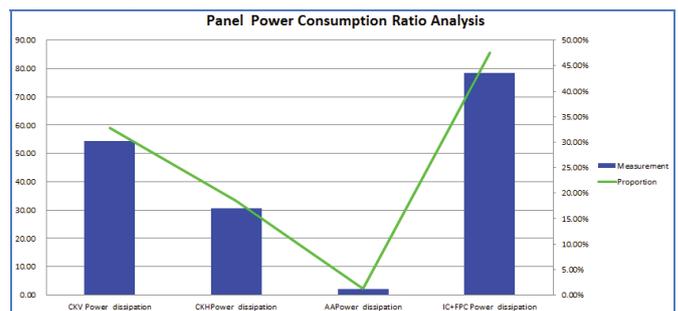


Figure 3. Panel Power Consumption Ratio Analysis

## 2.3 Power consumption simulation mode

### 2.3.1 The simulation model of capacitor charge and discharge is established

It is known that capacitor charge and discharge cause power consumption:

$$P_{switch} = nfcV^2$$

(Equation 6)

General consumer drive frequency is 60Hz, Set the driving voltage of each Panel -7~+8V, Timing set up with

3CKH=CKV, So knowing C is the key to solving this problem.

The switching voltage variation of the device is instantaneous, but does not mean that it cannot be captured. A device is made up of layers of layers that are stacked on top of each other, creating capacitance between them:

$$C = \frac{\epsilon S}{4\pi Kd} = \frac{\epsilon(W - L)}{4\pi Kd} \quad (\text{Equation 7})$$

Through Cleva simulation, we can extract the lateral capacitance between gate signal line and other membrane structures, and the forward capacitance can be obtained by the above formula.

### 2.3.2 simulation of through-current

The author designs a set of simulation circuits which can be seen on Figure 4, and uses ELDO to capture the charge amount of each TFT device in the output and non-output stages to analyze the source of the through-current in the integrated circuit, And we found that the sum of the two is equal to the total amount of charge going through H/L .,

$$Q = \int_0^t Idt \quad (\text{Equation 8})$$

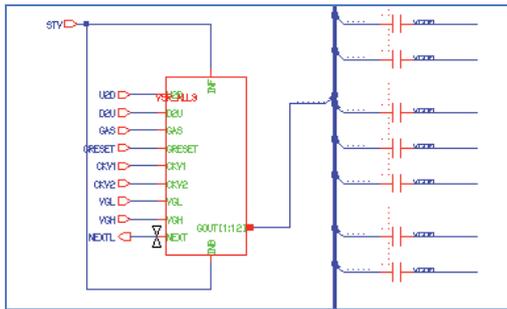


Figure 4. Simulation Circuits

Further analysis of the proportion relation shows that the three giants of the output level, Buffer\_3\_MP16, NAND gate and Latch, all have large proportion, but they are output once per frame, so their influence on the overall power consumption is small. On the contrary, in the non-output stage, since the revertor considers 2520 stage, the current ratio is more than 99%, which causes a huge loss to the overall circuit. The above high frequency signals cannot be connected to the reverse gate, otherwise the through-current will be very large. Result is shown on Figure 5.

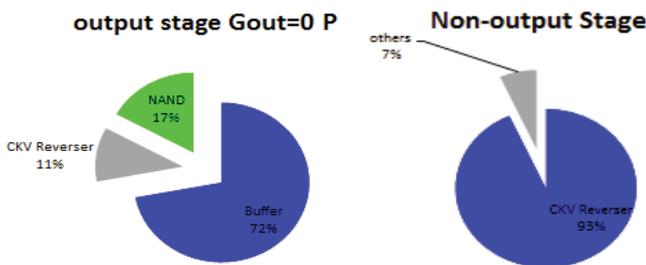


Figure 5. Power Consumption Ratio In Output And Non-output Stages

On the other hand:

Short circuit power consumption:

$$P_{short} = \frac{\int_0^t Idt}{T} V_{dd} = \frac{\int_0^t Idt}{T} (V_{dd} - V_{th}) \quad (\text{Equation 9})$$

Reduce the delay time of short current, The current peak value of CKV depends on the size of the device W/L. When the ratio is fixed, the compression of the device size also reduces the current impulse.

The author also designed a group of ELDO simulation for CKV current with the same peak value and different delay Time. Through the results of any case, the linear relationship between CKV inverse current and delay is often pointed out: (1) CKV delay prolongates, invert/NONE-gate current and Raising Time have the same trend; (2) Delay longer stage, both linear increase; (3) different CKV Delay results in equal peak height of inverters' current, while different widths result in large current, which shows a linear relationship with Delay time. Figure 6 expression

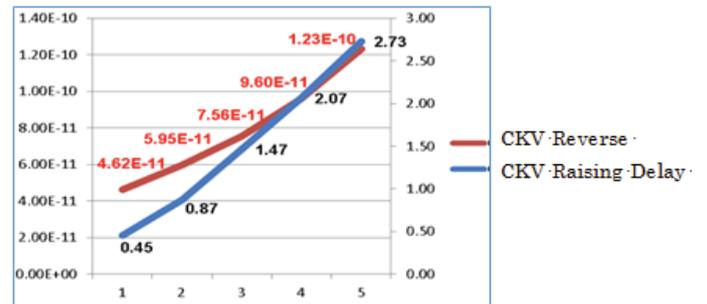


Figure 6. The Linear Relationship Between CKV Reverse Current And Ckv Raising Delay

### 2.4 consideration of power reduction of capacitor charge and discharge

Power consumption calculation formula is:

$$P_{demux} = V * I = V * (f * c) * \Delta c = fcV^2$$

f: pixel flip frequency;

V: supply voltage;

C: coupling capacitance

(Equation 10)

For consideration of f, the current RGB pixel design timing is RGBRGB, which can reduce the pulse frequency to 2/3 of the original and reduce the power consumption of Demux by 1/3 when converted into RBBRG.

For the consideration of c, the calculation formula of capacitance is as follows:

$$C = \frac{\epsilon S}{4\pi Kd} = \frac{\epsilon(W - L)}{4\pi Kd} \quad (\text{Equation 11})$$

To reduce power consumption, reduce C. C includes forward and lateral capacitance. However, when W\*L decreases, the carrier mobility will be affected. and the linear region equation calculation under Vds= 0.1v is usually defined:

$$I_{ds} = \mu_{eff} \frac{W}{L} C_{ox} [(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}]$$

(Equation 12)

On the premise of ensuring the stability of the device, appropriately reduce the size of L, at the same time, reduce W and maintain the ratio of W/L. This reduces the device size W/L to ensure  $I_{ds}$ , while reducing the W\*L area reduces the C. The 200/4 device can reduce the power consumption by 40% when reduced to 150/3; In addition, in the case of ensuring charging, reducing the pulse voltage can also significantly reduce the power consumption, the above three reduction measures can complement each other.

### 2.5 Design considerations for reducing through current

According to the above experimental and simulation results, to reduce the power loss caused by the through-current, we need to reduce the delay time of CKV, conduct quantitative compression for the device W/L, and avoid the large leakage flow caused by the high frequency signal connecting to the gate of the inverter in circuit design.

### 3 CONCLUSION

Based on the urgent demand of high PPI, high brightness and high frequency products, The designers of panel about power degradation design is severely tested. Through the design of experimental data and inverse model, we achieved a large degree of power degradation results: the power consumption of 120Hz products was about 1.2 times that of 60Hz products, and the power consumption of 90Hz products was about 1.09 times that of 60Hz products.

In this paper, the author mainly shares the thinking points of degradation of TFT devices in panel power consumption. For example, VSR design should reduce the impact brought by penetrating current, CKH voltage reduction or Demux TFT device size reduction is helpful to reduce Demux power consumption, and Fanout loading can consider same-sex interleave design? In addition, considering the process, the double-layer PLN design can effectively reduce the loading in area AA, etc.

In a word, the power consumption of integrated circuits has become an important indicator of the performance of electronic products in China, so it is particularly necessary to strengthen the research on the low-power design technology of integrated circuits.

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