P-type LTPS Gate Driver to Generate Simultaneous and Overlapping Progressive Outputs for High-Resolution AMOLED Displays

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ABSTRACT

A new low-temperature polycrystalline silicon (LTPS) gate driver is developed for active-matrix organic light-emitting diode (AMOLED) pixel circuits using simultaneous-emission (SE) driving scheme. Simulated results indicate that the proposed circuit successfully generates waveforms within the rising time of 0.6 μs under the RC loadings of 9.96 kΩ and 21.2 pF.

1 INTRODUCTION

Integrating gate driver circuit on glass substrate brings a lot of benefits, including low cost and overall compactness, so such technique has become a mainstream in industry [1]-[6]. Additionally, to pursue clear and vivid visual experience, high-resolution or high-frame-rate panels are required with high-speed-driving gate driver circuits [4]-[6]. Low-temperature poly-silicon thin-film transistors (LTPS TFTs) is more potential than amorphous silicon (a-Si:H) TFTs because LTPS TFTs have better driving capability and short response time. Thus, the size of LTPS TFTs can be designed smaller than that of a-Si TFTs for generating the output waveforms based on the same specification of panels, leading to a small layout area of LTPS gate driver circuits. Moreover, the parasitic capacitance is large in a-Si:H TFTs, increasing the instability factors of gate driver circuits and causing fluctuations of outputs. Also, a-Si:H TFTs have a degradation problem under stress, so the rising time or falling time of the output signals may become longer after long-term operation, resulting in poor image quality. In spite of the above-mentioned advantages of LTPS TFTs, the resistor-capacitor (RC) loading of row lines is still a big issue. In the progressive emission (PE) mode driving scheme, high-resolution panels require a short scan time for each row. Thus, pixel circuits may not be able to receive precise data voltage and finish complete compensation because of insufficient time. The RC loadings in row lines further distort the output pulses of gate driver circuits, resulting in higher error rates of the pixel circuits. To overcome this problem, several studies proposed the gate driver which can generate overlapping outputs. Lin *et al.* [5] proposed a simplified gate driver circuit with three-phase overlapping clock signals to realize overlapping outputs for being used in high-resolution and narrow-bezel applications. Also, a gate

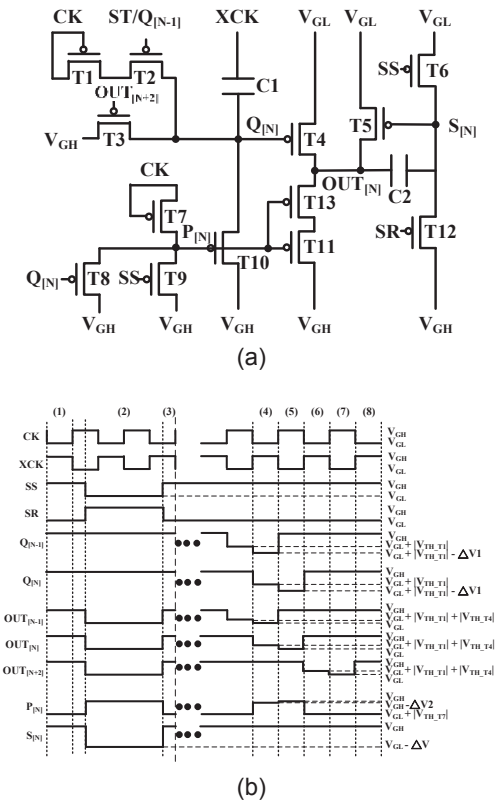

Fig. 1 Proposed pixel circuit. (a) Circuit schematic and (b) timing diagram of control signals.

driver circuit using a two-step-bootstrapping structure to generate high slew rate and overlapping outputs for high-resolution and high-frame-rate displays is developed [6]. The overlapping outputs of gate driver circuits expand the pulse width for driving pixels, so two rows of pixel circuits can operate in the same period, retarding the effect of RC loadings. For pursuing higher resolution displays, the simultaneous emission (SE) mode driving scheme tends to be a better way owing to longer compensation period than PE driving scheme. Since the RC loadings are inevitable and increases as the resolution becomes higher, the gate driver circuits with overlapping outputs for the data input period of SE driving scheme is needed.

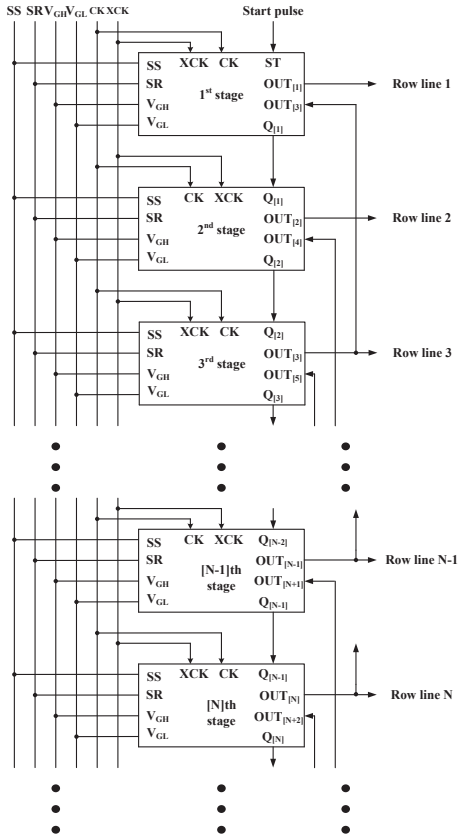

Fig. 2 Block diagram of proposed gate driver circuits.

This work proposes a p-type LTPS gate driver circuit with two inverted clocks and two controlling signals to generate two kinds of output signals for the SE driving scheme. By using the coupling effect from the RC loading of the row line, no extra voltage level is needed in the proposed circuit. Based on simulated results of the eight-stage proposed gate driver circuit, simultaneous and overlapping progressive signals for a 5.15-inch 240 Hz FHD display are successfully generated and the rising time of waveforms is within 0.6 μs.

2 EXPERIMENT

Fig. 1 presents the schematic of the proposed gate driver circuit and the relevant timing diagram. The circuit is composed of 13 p-type LTPS TFTs and two capacitors. C1 is used to bootstrap the $Q_{[N]}$ node for driving TFT (T4) to generate overlapping progressive waveforms. C2 is used for coupling voltage to $S_{[N]}$ node from a row line to fully turn on T5 and generate a simultaneous waveform. Two clock signals (CK and XCK) and two constant voltage powers (V_{GH} and V_{GL}) are used to drive the circuit. Besides, two control signals (SS and SR) are required for generating simultaneous outputs. Fig. 2 shows the block diagram of the proposed gate driver circuit. $OUT_{[N]}$ is the output node of the [N]th stage and used for resetting the [N-2]th stage. The circuit operation can be divided into eight periods and described as follows.

TABLE I
Parameters of Proposed Gate Driver Circuit

Parameter	Value	Parameter	Value
CK, XCK (V)	-8~8	$(W/L)_{T4, T11, T13}$ (μm/μm)	90/3
SS (V)	-8~8	$(W/L)_{T9}$ (μm/μm)	30/3
SR (V)	-8~8	$(W/L)_{T1, T2, T8, T10}$ (μm/μm)	15/3
V_{GH} (V)	8	$(W/L)_{OTHERS}$ (μm/μm)	3/3
V_{GL} (V)	-8	C1 (pF)	0.3
R_L (kΩ)	9.96	C2 (pF)	1
C_L (pF)	21.2		

In the first period, SS is at high and SR is at low. When CK goes to V_{GL}, the $P_{[N]}$ node is discharged to V_{GL} + $|V_{TH\_T7}|$ and turns on T10, T11 and T13. Therefore, the $Q_{[N]}$ and $OUT_{[N]}$ nodes are stabilized at V_{GH}. During the second period, SS turns to V_{GL} and SR turns to V_{GH}. The $S_{[N]}$ node is discharged to a low voltage for turning on T5 and the $OUT_{[N]}$ node starts discharging. Since the $OUT_{[N]}$ node connects to the whole [N]th row, the RC loadings of the row line causes the $OUT_{[N]}$ node to be discharged slower than the $S_{[N]}$ node. As the $S_{[N]}$ node is discharged to V_{GL} + $|V_{TH\_T6}|$, T6 is turned off automatically and T5 is still turned on for discharging the $OUT_{[N]}$ node. Thus, $S_{[N]}$ node becomes floating and is coupled to V_{GL} - ΔV. Therefore, T5 is at the linear region, and the $OUT_{[N]}$ node is able to reach V_{GL}. At the same time, T9 which is designed to be larger than T7 is turned on, and the $P_{[N]}$ node is kept at a high voltage to turn off T11 and T13 for a stable output. Next, in the third period, SS is turned back to V_{GH} and SR is turned back to V_{GL}. T12 is turned on for keeping the $S_{[N]}$ node at V_{GH}, and T5, T6 and T9 are turned off. When CK goes to V_{GL}, the $P_{[N]}$ node is discharged to V_{GL} + $|V_{TH\_T7}|$ through T7. Therefore, T10, T11 and T13 are turned on to stabilize the $Q_{[N]}$ and $OUT_{[N]}$ nodes at V_{GH}. In the fourth period, the $Q_{[N-1]}$ signal from the previous stage changes to low. The $Q_{[N]}$ node is discharged to V_{GL} + $|V_{TH\_T1}|$ through T1 and T2. Therefore, T4 is turned on for discharging the $OUT_{[N]}$ node and the overlapping output is realized. In addition, T8 is designed to be larger than T7, so the $P_{[N]}$ node is charged at a high voltage of V_{GH} - ΔV2 even though T7 is turned on. Therefore, T10, T11 and T13 are turned off so that the $Q_{[N]}$ and $OUT_{[N]}$ nodes are prevented from being charged. In the fifth period, XCK changes from high to low. Since the $Q_{[N-1]}$ signal changes to V_{GH}, the $Q_{[N]}$ node becomes floating and is coupled to a lower voltage of V_{GL} + $|V_{TH\_T1}|$- ΔV1. Therefore, T4 can be operated at the linear region and V_{GL} is completely transmitted to the $OUT_{[N]}$ node. Additionally, T8 is turned

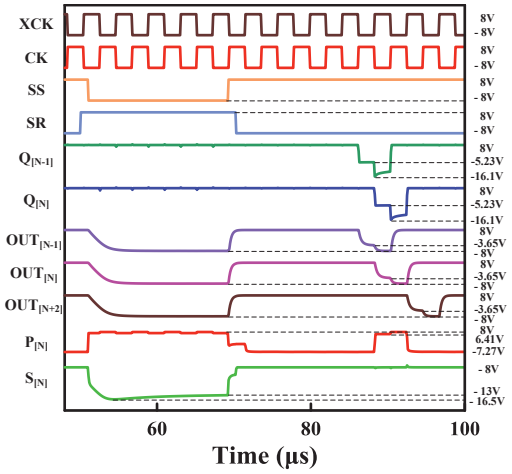

Fig. 3 Simulated waveforms of clock signals, control signals, $Q_{[N-1]}$, $Q_{[N]}$, $OUT_{[N-1]}$, $OUT_{[N]}$, $OUT_{[N+2]}$, $P_{[N]}$, and $S_{[N]}$.

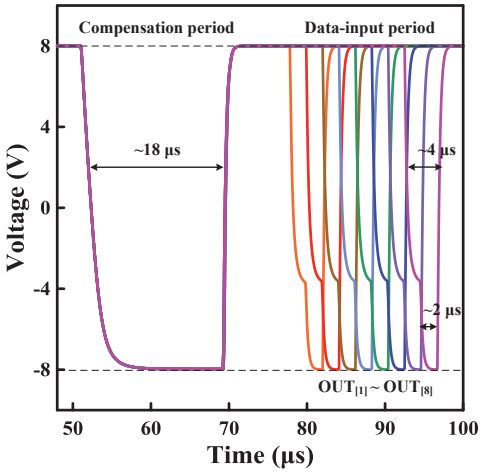

Fig. 4 Simulated output waveforms from first to eighth stage of proposed gate driver circuit.

on, and CK changes to high so that $P_{[N]}$ node is charged to V_{GH}. T10, T11 and T13 are turned off to prevent the $OUT_{[N]}$ node from being charged. In the sixth period, XCK turns back to V_{GH} and the $OUT_{[N+2]}$ signal from next two stage becomes low. Thus, the $Q_{[N]}$ node is charged through T3 for turning off T4. Meanwhile, CK changes to V_{GL} and the $P_{[N]}$ node is discharged to V_{GL} + $|V_{TH\_T7}|$. Therefore, T10, T11 and T13 are turned on for charging the $Q_{[N]}$ and $OUT_{[N]}$ nodes. In the seventh period, the $OUT_{[N+2]}$ node is still at V_{GL} and the $Q_{[N]}$ node is kept at V_{GH} for turning off T4. The $P_{[N]}$ node remains at V_{GL} + $|V_{TH\_T7}|$ because there is no charging path for the $P_{[N]}$ node. Thus, T10, T11 and T13 are turned on for keeping the $Q_{[N]}$ and $OUT_{[N]}$ nodes at V_{GH}. Subsequently, in the eighth period, the $OUT_{[N+2]}$ signal changes to V_{GH}, and T3 is turned off. The $P_{[N]}$ node is periodically set to V_{GL} + $|V_{TH\_T7}|$ as CK changes to V_{GL}, stabilizing the $Q_{[N]}$ and $OUT_{[N]}$ nodes at V_{GH}.

3 RESULTS

To verify the functionality of the proposed gate driver circuit, HSPICE simulator and a p-type LTPS TFT model are used. Table I lists the designed parameters, including the voltage swings of clock signals (CK and XCK) and controlling signals (SS and SR), the voltage levels of constant power signals (V_{GH} and V_{GL}), and the size of each TFT (T1-T13). To meet the requirements of 5.15-inch 240 Hz Full HD (1080×1920) panels, the pulse width of CK and XCK is set to 2 μs, and the RC loadings in row lines are set to 9.96 kΩ and 21.2 pF.

Fig. 3 plots the simulated waveforms of clock signals, control signals, $Q_{[N-1]}$, $Q_{[N]}$, $OUT_{[N-1]}$, $OUT_{[N]}$, $OUT_{[N+2]}$, $P_{[N]}$, and $S_{[N]}$. When SS turns to -8 V and SR turns to 8 V, $S_{[N]}$ node is coupled to -16.5 V through C2. Therefore, T5 is in the linear region and V_{GL} can be fully transmitted to $OUT_{[N]}$. As shown in Fig. 3, $OUT_{[N-1]}$, $OUT_{[N]}$ and $OUT_{[N+2]}$ simultaneously output -8 V to the row lines. At the same time, $P_{[N]}$ and $Q_{[N]}$ are at about 8 V to prevent $OUT_{[N]}$ from being charged. As SS changes to 8 V and SR changes to -8 V, $P_{[N]}$ decreases to about -1.2 V and $OUT_{[N]}$ can be raised up to 8 V. When $Q_{[N-1]}$ is coupled to -16.1 V, $Q_{[N]}$ node is discharged to -5.23 V. Thus, T4 is turned on and starts discharging $OUT_{[N]}$. Next, XCK turns from 8 V high to -8 V, and $Q_{[N]}$ is coupled to -16.1 V. Therefore, T4 is operated at the linear region and $OUT_{[N]}$ can be discharged to -8 V. Additionally, $P_{[N]}$ is kept at higher than 6.41 V for turning off the pull-up circuit when $OUT_{[N]}$ is discharged to -8 V. Lastly, when the reset signal $OUT_{[N+2]}$ from the [N+2]th stage changes to -8 V, $Q_{[N]}$ and $OUT_{[N]}$ are raised up to 8 V and remained at 8 V until both SS and SR change state again in the next frame. Fig. 4 demonstrates the simulated output waveforms of continuous eight stages. As the pixel array is operated during the compensation period, $OUT_{[1]}$ to $OUT_{[8]}$ are simultaneously discharged to -8 V for about 18μs. Afterward, $OUT_{[1]}$ to $OUT_{[8]}$ are sequentially generated for the data-input period of the pixel array. The pulse width of overlapping outputs are about 4 μs for pixels to receive data voltage, able to fulfill pre-charge function for 240 Hz FHD panels. Table II shows the rising and falling times of $OUT_{[6]}$. The rising times for both the compensation period and the data-input period are less than 0.6 μs, ensuring the effectiveness of the proposed gate driver circuit.

TABLE II
Rising and Falling Times of $OUT_{[6]}$

Compensation period		Data-input period
Falling time	Rising time	Rising time
0.86 μs	0.59 μs	0.58 μs

4 CONCLUSIONS

In this work, a p-type LTPS gate driver circuit is proposed for driving SE mode AMOLED pixel circuits. By utilizing the coupling effect from the row lines, the simultaneous outputs are able to be discharged to VGL without additional low voltage level. Furthermore, two inverted clock signals and a storage capacitor is designed for overlapping progressive outputs, so pixels in panels can achieve pre-charging function for the accurate data voltage in high-resolution panels. Simulated results show that eight-stage gate driver circuit successfully generates the output waveforms within the rising time 0.6 μs, confirmed its effectiveness for use in 5.15-inch 240 Hz FHD displays.

CONCLUSIONS

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