Highly Reliable a-IGZO TFT Gate Driver Circuit to Suppress Threshold Voltage Shift of Pull-down TFT

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ABSTRACT

We present highly reliable gate driver circuit using AC-driven method of a pull-down TFTs. Two pull-down TFTs are driven with duty ratio of 33.3% and 66.7%, respectively, VOUT discharge completely. The proposed circuit can minimize coupling noise by discharging the Q and VOUT node constantly except for output period.

1 INTRODUCTION

The a-Si:H TFT, which has advantage of low cost and low temperature processing, is widely used in the display industry [1], [2]. However, the most serious problem of the a-Si:H TFT is the low mobility. The low mobility makes difficult to implement high-speed driving circuit and high-resolution display. Recently, oxide TFT has been noted for its higher mobility and low off-current compared to a-Si:H TFT [3], [4]. The high electron mobility characteristics of the oxide TFT enable high resolution panel implementation through high speed driving [5]. In addition, the low leakage current characteristic realizes a low scan rate operation without changing the image quality, thereby display power consumption can be reduced [6]. So, the oxide TFT enables to be implemented in large screen and high-resolution displays. Nevertheless, the oxide TFT has a serious problem such as characteristics variation of the TFT due to the bias stress, and such a characteristic variation of the TFT can influence on the circuit operation [7-9].

Meanwhile, gate driver circuit is composed of input TFTs, pull-down TFTs, and pull-up TFTs which are responsible for stable voltage transfer to each pixel. In this case, the pull-down unit is always turned on to maintain the VOUT at the low voltage, except for output period. Therefore, the pull-down TFT is driven by DC type. However, DC-type drive will result in continuous bias stress for the pull-down unit, resulting in deterioration of the TFT. The deterioration of the TFT and the change in electrical characteristics (threshold voltage shift) directly affect the stability of the circuit [10]. To prevent this phenomenon, many groups are proposed circuit structures to ensure the stability of the circuit [11-13]. As one of the methods to ensure stability, a circuit using AC-driven of a pull-down unit is presented. However, if the pull-down unit couldn't discharge the output to 100% as shown in [13], output fluctuation may occur.

Therefore, this paper proposes a high reliable gate driver circuit that uses two pull-down TFTs which have 33.3% and 66.7% turn-on duty ratio, respectively, therefore, VOUT can be pulled down with 100% duty ratio. In addition, the Q node can be also discharged at 100% except for output period. This stable implementation of Q node operation can reduce coupling noise caused by CLK.

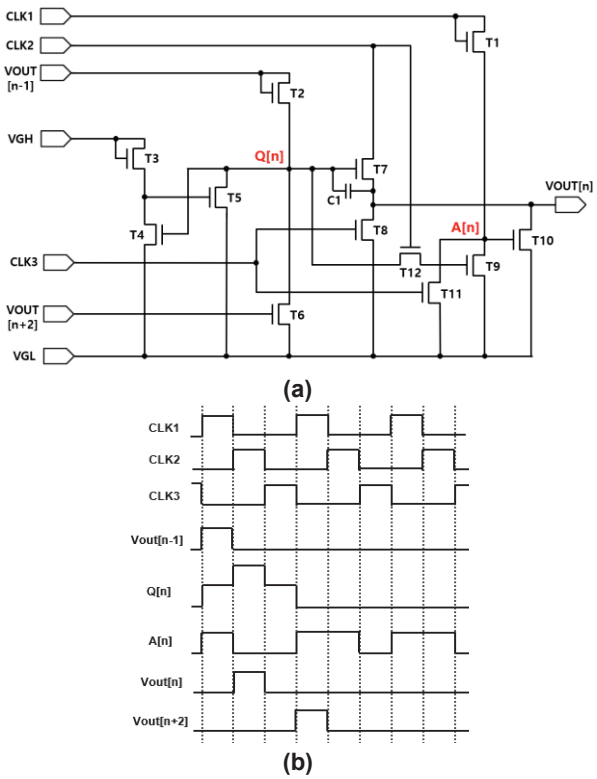


Fig. 1 (a) proposed gate driver circuit (b) timing diagram

2 OPERATION

Fig. 1 (a) shows the proposed gate driver circuit schematic and (b) is timing diagram. The proposed circuit consists of twelve TFTs and one capacitor. The circuit has three clock signals and two sources of DC

voltages, VGL of -5V and VGH of +28V, are applied to circuit. Circuit operation can be divided into four sections.

2.1 Pre-charging

The first section, VOUT[n-1] becomes VGH, the Q node is pre-charged through T2. So, T4 and T7 are turned on to the VOUT[n] node at VGL. In addition, the Q node voltage cannot be transferred to the gate node of T9. Therefore, A node does not generate the through current due to CLK1.

2.2 Bootstrapping

The second section, CLK2 is up to VGH. Therefore, the Q[N] node is bootstrapped through the capacitive coupling by C1. So, the driving capacity of T2 is increased by the gate voltage rise and the stable VGH voltage is transmitted to the VOUT[n] node. And, T4 is in the on-state to ensure that T5 is completely turned off, so, preventing the discharge of the Q[n].

2.3 Reset

In the third section, CLK3 becomes VGH. However, since T6 is off, the Q node voltage remains VGH. Therefore, the VOUT node is discharged through T7 which is buffer TFT. So, we can improve falling time.

2.4 Low-holding

After the output duration, the Q[n] and OUT[n] nodes must be maintained at VGL. Meanwhile, when CLK is applied to the drain node of T7, fluctuation can be occurred to Q and VOUT node due to the capacitive coupling of T7. Therefore, in the fourth section, the VOUT [n + 2] becomes VGH, and Q node is discharged through T6. Thus, T4 is turned off and T5 is turned on by VGH. Therefore, after the output section, the Q node is continuously discharged through T5 to prevent voltage fluctuation for Q and VOUT node. In addition, CLK1 becomes VGH, VOUT discharges to 66.7% through T10. When CLK3 becomes VGH, node A is discharged through T11, and VOUT is discharged to 33.3% through T8. Thus, The VOUT node is discharged at 100% duty ratio without any floating period. As a result, the stability of the gate driver circuit is ensured.

3 RESULTS

Fig. 2 shows the I-V transfer curve of the a-IGZO TFT model used in the proposed circuit. The channel width of the TFT is 50μm, the channel length is 5μm and the threshold voltage is +1.5V. The proposed circuit is simulated by Smart Spice with oxide TFT (Level = 35). The zero-bias-threshold voltage (V_{TO}) was set at +0.0285V and the flat-band voltage (V_{FB}) was set at -0.280V. The threshold voltage was changed through V_{TO} and V_{FB}. Table. 1 shows the design parameters of the proposed circuit. CLK swing from -5V to +28V, VGH is +28V, and VGL is -5V. 1line time is 7.7μs based on Full-HD resolution (FHD), and the CLK frequency is 43.3kHz.

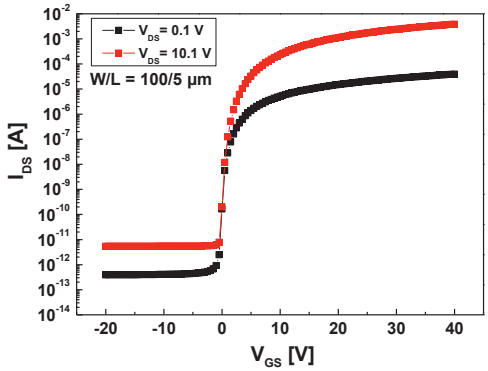


Fig. 2 I-V characteristics of a-IGZO TFT model

Table. 1 design parameters of the proposed gate driver circuit

Proposed Circuit			
L	5μm	T9, T12	10μm
T1	80μm	C1	1 pF
T2, T5, T6	50μm	CLK voltage	-5 to +28V
T3, T11	5μm	CLK Duty Ratio	33.3%
T4	160μm	VDD	+28V
T7	700μm	VSS	-5V
T8, T10	200μm		
L=TFT Length, W=TFT Width CLK Frequency 43.3kHz, Line Time 7.7μs (FHD Resolution, Frame Frequency 120Hz)			

Fig. 3 shows the simulation results of Q, A, and VOUT nodes of the proposed circuit. The Q node is pre-charged to +26.2V and bootstrapped to +53.0V. Therefore, the VOUT node received +28V stably. A node operates T10

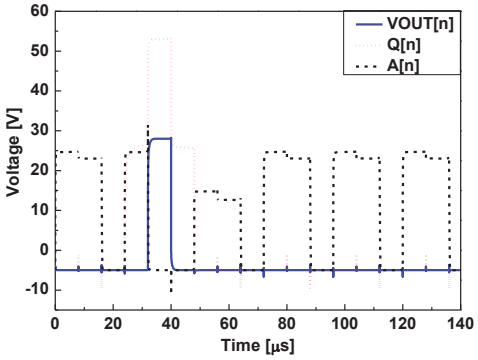
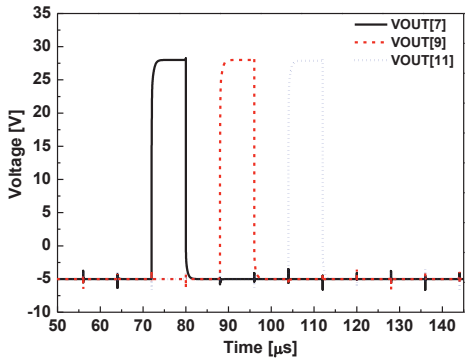


Fig. 3 The simulated waveform of VOUT[n], Q[n], and A[n]

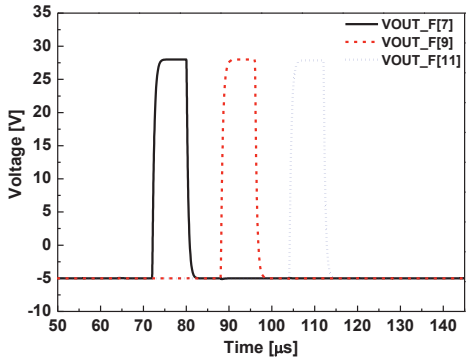
by maintaining +25.47V with 66% duty ratio except CLK3 input section.

Fig. 4 (a) and (b) show the VOUT nodes of the 7th, 9th and 11st stages of 15 stages. RC value for row line is

120pF, 5.4kΩ, and VOUT_F[n] is the VOUT node farthest from RC road [14]. In simulation result, the VOUT node received +28V stably in all three stage. In addition, in Fig. 3 (b), the rising / falling times of the 7th, 9th, and 11st outputs were 0.984μs / 0.916μs, 0.990μs / 0.918μs, and 0.993μs / 0.919μs. Therefore, the proposed circuit can be driven stably at FHD resolution.



(a)



(b)

Fig. 4 (a) The simulated VOUT[n] waveform of 7th, 9th and 11st stage (b) The simulated VOUT_F[n] waveform of 7th, 9th and 11st stage

Fig. 5 shows the variation of rising / falling time when the threshold voltages of all TFTs were shifted from +0.5V to +6.5V. At the threshold voltage of +6.5V, the rising / falling time is 1.206μs / 0.956μs which is increased by 24% / 5% compared to 0.968μs / 0.907μs at +0.5V. Therefore, we confirmed that the proposed circuit can operate normally within +6V range.

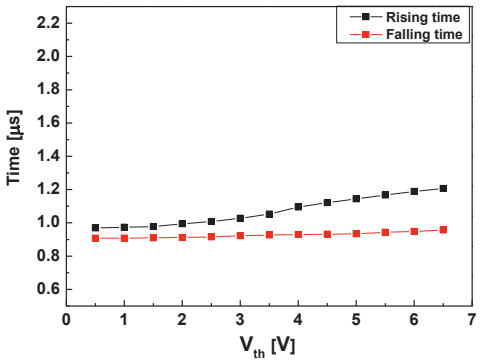


Fig. 5 The rising / falling time characteristics according to threshold voltage variation

4 CONCLUSIONS

We propose highly reliable gate driver circuit using AC-driven method of pull-down unit. Two pull-down TFTs are alternately driven with a duty ratio of 33.3% and 66.7%, respectively, reducing the bias stress on the pull-down TFT. Therefore, we can expect that the threshold voltage shift for the pull-down TFT will decrease. In addition, coupling noise caused by CLK pulse is minimized by stable operation of the pull-up unit. According to the simulation results, the outputs of the 7th, 9th and 11st stages of 15 stages received +28V stably. The rising / falling time of each stage was within 1μs. In addition, even if the threshold voltage is shifted by +6V (actual threshold voltage= +6.5 V), the rising / falling time is 1.251μs / 0.956μs. As a result, proposed circuit can operate stably at FHD resolution.

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