Novel Driving Methods of Gate Driver Circuit for Depletion Mode Oxide TFTs

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Keywords: Gate Driver Circuit, Thin-Film Transistor, Depletion Mode, Threshold Voltage, Reliability

ABSTRACT

We introduce novel driving methods of pull-down unit in a gate driver circuit for enhancement and depletion mode a-IGZO thin-film transistors (TFTs). Using 3T1C diode connection structure, our circuit can compensate for V_{TH} of pull-down unit in the enhancement mode and can be normally operated in the depletion mode.

1 INTRODUCTION

Amorphous indium gallium zinc oxide thin-film transistor (a-IGZO TFT) is one of the promising candidates for various next-generation display panels due to high mobility, low off-current level, and high uniformity compared to a-Si:H TFT [1-3]. In the IGZO structure, the crystal structure of InO_2 can increase the electron mobility because indium is formed in the 5s orbitals and oxygen is formed in the 2p orbitals in the band structure [4]. In addition, IGZO has a large bandgap, which can transmit the visible light due to its transparent property. Therefore, IGZO has good electrical and optical characteristics. However, the electrical performance of an IGZO TFT can be degraded by the electrical bias stress or illumination stress. Moreover, the IGZO TFT can be operated in the depletion mode with a negative threshold voltage [5]. When it is applied to an integrated circuit, such as gate driver and pixel compensation circuit, circuit malfunction can occur due to leakage current path. In this paper, we introduce novel driving methods of the gate driver circuit for both enhancement mode and depletion mode a-IGZO TFTs. Despite the same circuit structure, the proposed circuit can be operated with different driving methods for the enhancement and depletion modes, respectively. The result shows that the proposed circuit has a large V_{TH} shift margin from -7 V to +11 V.

2 PROPOSED GATE DRIVER CIRCUIT

Fig. 1 (a) and (b) show the schematic for proposed gate driver circuit for 1 stage, and the voltage timing diagram. The proposed circuit is composed of thirteen TFTs, two capacitors, two low-voltage signals (VGL1 and VGL2), and two CLK bus lines (CLK and CLKB). All CLKs and V_{OUT} signals are operated within a swing range from -5 V to +28 V. Moreover, Carry signals are operated with the swing

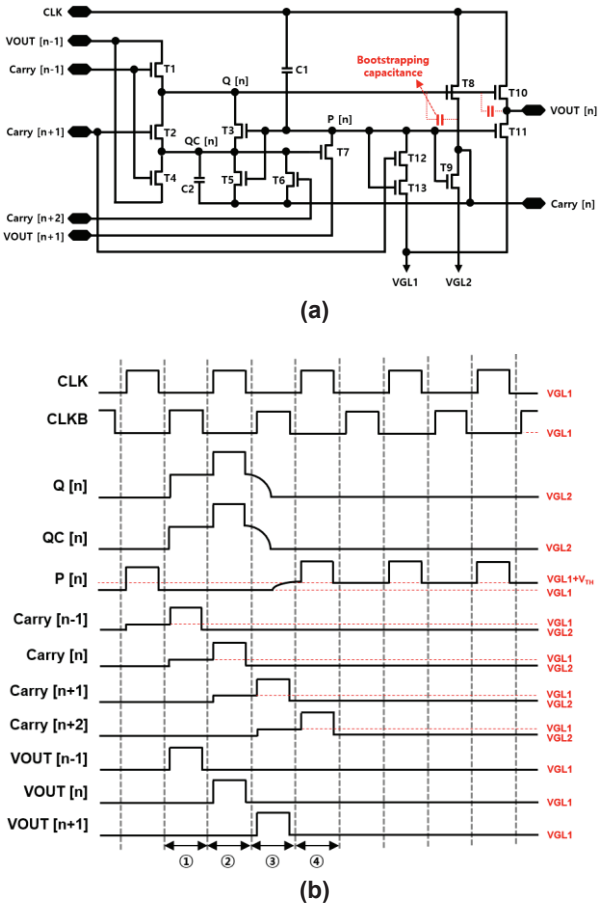

Fig. 1 Proposed gate driver circuit to realize the novel V_{TH} compensation methods for both enhancement- and depletion-mode a-IGZO TFTs: (a) circuit schematic and (b) timing diagram

range from -13 V to +28 V. For application to the depletion mode IGZO TFTs, we designed a QC node into the new circuit first. The V_{OUT} degradation can be generated in the depletion mode IGZO TFTs because the TFT enters the turn-on state even when the V_{GS} value is 0 V. The Q node leakage current paths are three points (T1, T2, and T3). To solve this problem, the QC node can prevent the leakage current path for Q node

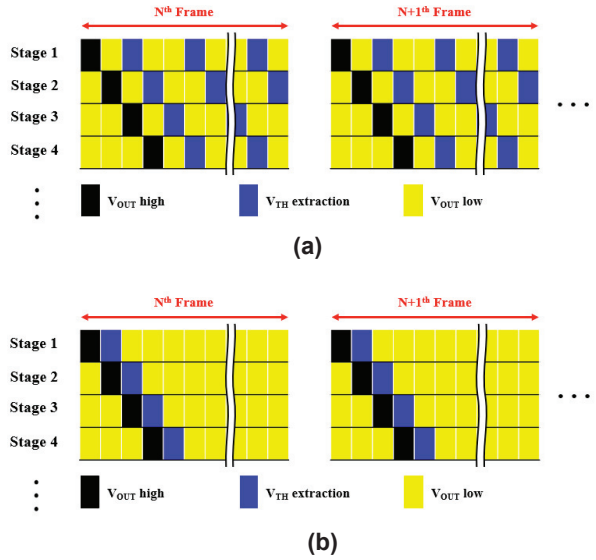

Fig. 2 Method of threshold voltage extraction for the pull-down unit: (a) threshold voltage extraction method of conventional circuit and (b) threshold voltage extraction method of proposed circuit

because the V_{GS} value of T2 and T3 in the bootstrapping period is less than 0 V, based on the Q node. The leakage current path of T1 can also be eliminated by using Carry n-1 signal (V_{GS_T1}= -8 V). As a result, pre-charging and bootstrapping voltage of the Q node can be respectively maintained by VGH-V_{TH_T1} and VGH-V_{TH_T1}+ΔV for both enhancement mode and depletion mode IGZO TFTs.

Fig. 2 (a) shows the conventional V_{TH} extraction method for the pull-down unit [6]. The conventional V_{TH} compensation circuit for the pull-down unit should have three CLK signals because the V_{TH} compensation operation is composed of three parts: initialize period, V_{TH} extraction period, and V_{TH} compensation period. When the depletion-mode IGZO TFT is applied to the conventional V_{TH} compensation circuit structure, however, the V_{TH} extraction and operation of the pull-down unit are impossible because low voltage is applied to the pull-down unit due to diode connection structure. If the diode connection structure of the pull-down unit is formed by CLK, the V_{GS} value of pull-down unit is 0 V; it means that pull-down TFT is continuously in the turn-on state. As a result, the V_{TH} extraction becomes impossible. To solve the V_{TH} extraction problem for the depletion mode IGZO TFTs, we newly designed the extraction time using a similar conventional circuit structure. Fig. 2 (b) shows our proposed V_{TH} extraction method for the depletion-mode IGZO TFTs. In the proposed method, the V_{TH} extraction is only one time based on one frame time. In section 3 of Fig. 1 (b), T7, which is the input TFT, is turned on by the QC node and V_{OUT} n+1. Therefore, T13 is in the turn-on state for a short time, which can extract V_{TH} of T13 because T12 is turned on by Carry n+1. At this time, the leakage paths for the P node are not generated because all the V_{GS} values of T7 and T12 are less than 0 V despite V_{GS} of T13 being 0 V. After the V_{TH} extraction time, the V_{TH} compensation and extraction holding are repeated by CLK and C1. As a result, our circuit can compensate V_{TH} of the pull-down unit in the enhancement mode and can be normally operated in the depletion-mode IGZO TFTs.

3 RESULTS AND DISCUSSIONS

Fig. 3 shows the simulated voltage waveforms for enhancement mode IGZO TFTs. Fig. 3 (a) and (b) shows the Q node, P node, and V_{OUT} characteristics for the enhancement mode IGZO TFTs with different operation time. In the proposed circuit, the shift margin of positive V_{TH} is +11 V (actual V_{TH}= +11.5 V). The result indicates that the extracted V_{TH} of pull-down unit is +11.5 V because the P node voltage is +6.5 V in the V_{TH} extraction period (VGL1= -5 V) as shown in Fig. 3 (a). Next, the P node is driven by AC-type depending on the CLK voltage. We can know that driving voltage of pull-down unit (P node) increases to compensate the pull-down unit degradation after V_{TH} extraction period. Therefore, the ripple voltage of the V_{OUT} node can be successfully suppressed and be obtained uniform V_{OUT}

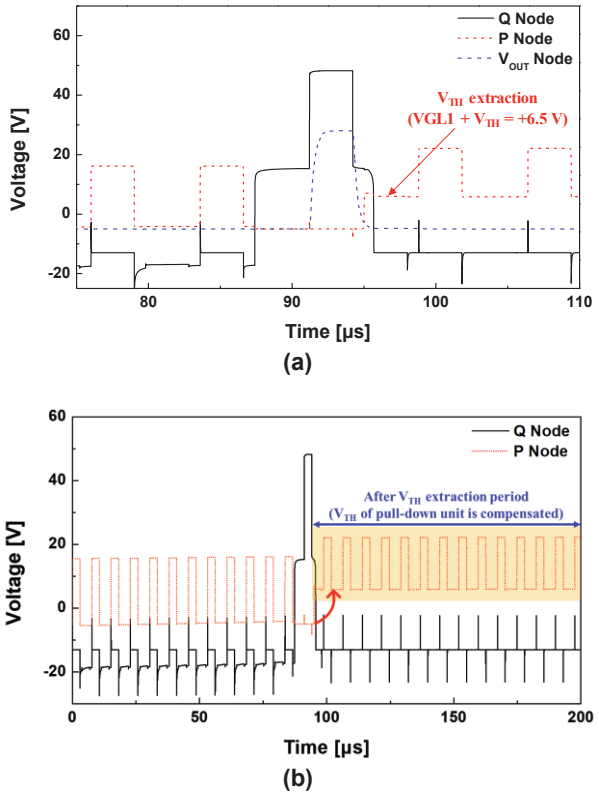

Fig. 3 The simulated voltage waveforms for enhancement mode oxide TFTs: (a) Q, P, and V_{OUT} node voltage waveforms from 75 μs to 110 μs at ΔV_{TH}= +11 V (V_{TH}= +11.5 V) and (b) Q and P node voltage waveforms from 0 μs to 200 μs

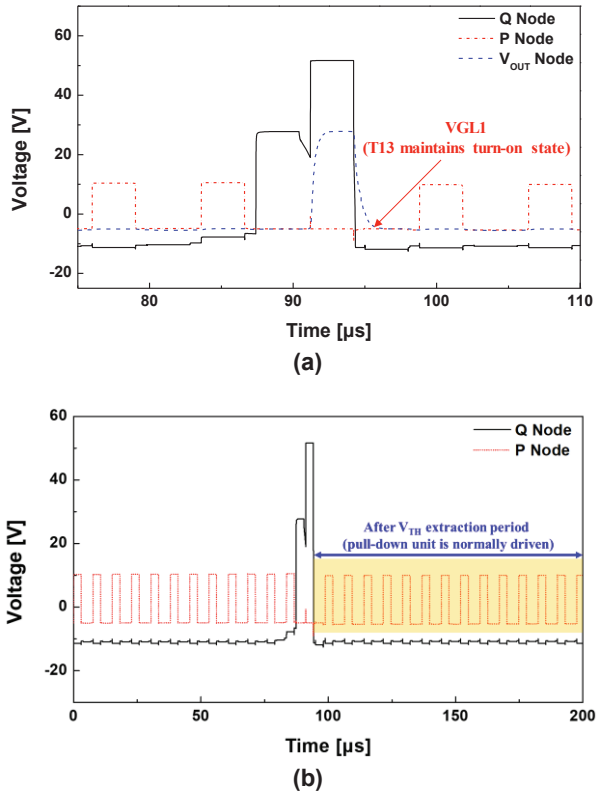

Fig. 4 The simulated voltage waveforms for depletion mode oxide TFTs: (a) Q, P, and V_{OUT} node voltage waveforms from 75 μs to 110 μs at ΔV_{TH}= -7 V (V_{TH}= -6.5 V) and (b) Q and P node voltage waveforms from 0 μs to 200 μs

characteristics by the V_{TH} compensation of the pull-down unit. The V_{OUT} output characteristics show that the output level, rising time, and falling time are +28 V, 0.62 μs, and 0.62 μs, respectively. The rising time and falling time are almost same in the enhancement mode IGZO TFTs because the charging or discharging of the V_{OUT} node is performed by T10, which is the same as the TFT using Q node. Therefore, the proposed circuit can realize uniform output pulse to obtain high reliability.

Fig. 4 (a) and (b) show the Q node, P node, and V_{OUT} characteristics for the depletion mode IGZO TFTs. The simulation was performed when the V_{TH} of all TFTs is -7 V (actual V_{TH}= -6.5 V), which is the largest negative V_{TH} margin, similar to the enhancement mode. The result shows that the P node is maintained at -5 V in the V_{TH} extraction period because V_{GS} for T13 is 0 V. In the reset and V_{TH} extraction period, Q node, QC node, and V_{OUT} reset are performed by T2, T5, and T6, respectively. It indicates the application of different operation principles for the negative and positive the threshold voltages of IGZO TFT despite the same circuit structure. Therefore, the circuit can be normally driven without any voltage degradation. The V_{OUT} characteristics show that the output level, rising time, and falling time are +27.8 V, 0.57 μs, and 0.96 μs, respectively. Although the output level and falling time degraded slightly, the circuit operation was conducted without any difficulty. Consequently, we can obtain a large V_{TH} tolerance in the proposed circuit under the V_{TH} shift conditions from -7 to +11 V.

4 CONCLUSIONS

In this work, we proposed novel driving methods for the pull-down unit in the gate driver circuit for both enhancement and depletion modes a-IGZO TFTs. To realize high circuit reliability, it is necessary to adopt a V_{TH} compensation structure for pull-down units. However, a diode connection structure to compensate V_{TH} for pull-down units cannot be operated in the depletion mode IGZO TFTs because V_{GS} of pull-down unit is always 0 V. It can cause circuit malfunction because V_{OUT} voltage is discharged by pull-down unit in the Q node pre-charge and bootstrapping period. To solve this problem, we adopted the V_{TH} extraction period once for each frame time. Consequently, the proposed circuit was found to compensate the V_{TH} of the pull-down unit in enhancement mode and can be normally operated in the depletion mode. The result shows that all V_{OUT} voltage waveforms were maintained at +28 V under the V_{TH} shift conditions varying from -7 V to +11 V. Additionally, the rising time and falling time were found to be lesser than 0.62 and 0.96 μs, respectively.

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