Study on Top-Gate Self-Aligned InGaZnO TFTs on PI Substrate

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Abstract

We discussed the effect of polyimide substrate on TFTs, the water from polyimide diffused into IGZO which deteriorated device characteristic. By reducing hydrogen content in GI we optimized device characteristic, and GI 1step deposition is more stable. Finally, we did the static bending and dynamic test, TFTs keep good stability.

1 Introduction

Flexible displays have significant growth in recent years for new applications like foldable、rollable、stretchable display. Oxide semiconductors (for example IGZO) of high mobility, low fabrication temperature and good machine stability are great for fabricating flexible backplane[1], and for micro LED, top-gate self-aligned(TG SA) structure is necessary to reduce parasitic capacitance between gate and source/drain electrodes. Polyimide has good thermal stability, dimensional stability, solvent resistance and smooth surface as flexible substrate[2], most of flexible displays are fabricated on PI. However, polyimides are known to absorb water , and the moisture absorption in polyimide is dependent on the component and structure[3,4], absorbed water in PI may be released and diffused into upper layers like SiOx and a-IGZO. H2O molecules can induce extra electron carriers and cause Vth instability during positive bias stress[5,6].

In this paper, we used a 10um PI of 2.2% water absorbance as substrate, and discussed the effect of PI on TG-SA TFTs properties . Then we optimized device characteristic on PI glass. Finally , we did the static bending and dynamic test after lifted-off , TFTs on PI keep good PBTS stability.

2 Experiment

The structure of top-gate self-aligned a-IGZO TFTs is showed in **Fig. 1.** They were fabricated on Gen 4.5 glass. Firstly, a SiNx and SiOx stacked layer was deposited on substrate (PI glass or bare glass) as barrier layer to isolate moisture diffusion[7]. Secondly, a light-shielding metal (LS) was deposited and patterned. Then, a SiOx buffer layer was deposited by plasma enhanced chemical vapor deposition (PECVD). After annealed a a-IGZO layer was deposited by AC sputter, and defined through photolithography and wet etching after annealed. SiOx layer was deposited by PECVD as the gate insulator (GI) . Mo/Al/Mo metal layers were deposited using DC sputter as the gate layer. Gate and GI layer were continuously patterned to form top-gate self-aligned structure. Plasma treatment was applied for creating n+ IGZO S/D ohmic contact. After inter-layer dielectrics deposition (ILD), Mo/Al/Mo metal layers were deposited and patterned as the source (S) and drain (D). Devices fabrication were finished by passivation (PV) layer deposition. Keithley 4200-SCS semiconductor parameter analyzer was used to measure device electrical properties in the dark. The positive bias stress stability (PBTS) tests in this paper were all the same condition: +30V VG bias under 60℃ for 2000s.

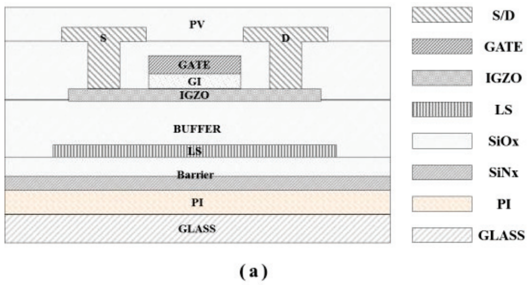

Fig. 1 The structure of TG-SA IGZO TFT on PI substrate

3 Results and discussion

To investigate the effect of substrate on the TFT characteristics, we measured the Id-Vg transfer curve at different sites on Gen. 4.5 bare glass (sample A) and PI glass (sample B) with same barrier and other process conditions. Then, GI deposition condition was optimized with 2steps deposition (sample C) and 1step deposition (sample D), Id-Vg transfer curve was measured. The TFTs characteristics are showed in **Table 1**. For micro LED, like OLED, is current driving , the electrons are easy trapped by act-GI interface/GI defects[8], so the PBTS was also measured. Finally , after laser lifted off (LLO) process ,we measured PBTS in the static bending state with a radium of 0.5mm and after dynamic test with a radium of 5cm for 5000cycles.

Table 1 The characteristic of sample A/B/C/D

Sample	A	B	C	D
Mobility（cm^2/Vs）	12.90	13.60	10.90	11.35
SS（V/decade）	0.34	0.48	0.36	0.38
Vth（V）	-0.48	-3.69	1.58	0.01
$\triangle V_{th}$（V）	0.72	8.54	1.04	0.67

3.1 Effect of substrate

Sample A and sample B were fabricated with the same condition but on different substrate, sample A was on the bare glass and sample B was on the PI glass. **Fig. 2** is the IdVg curve, sample B on the PI glass TFT Vth was obviously negative shift comparing with sample A. During anneal and other high temperature process, like CVD, absorbed water in PI was released gradually and diffused into a-IGZO, H2O-related tarps active as donor like traps, witch induced extra electron carriers and cause Vth negative shift [5,9,10]. So it's important to reduce the hydrogen content to optimize electrical property on PI glass.

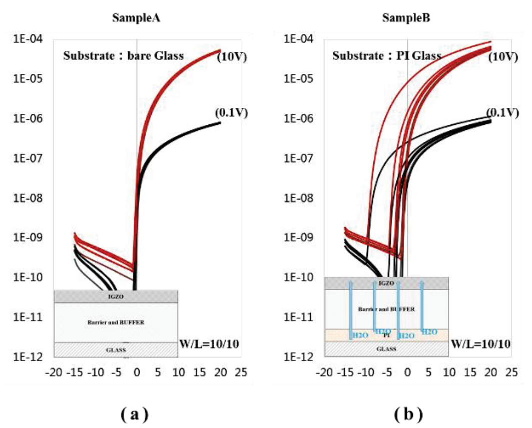

Fig. 2 The Id-Vg curve at different sites with (a)TFTs on bare glass substrate (b)TFTs on PI glass substrate with same process conditions.

3.2 GI deposition condition

Gate insulation layer directly contacts with active layer, the defect at interface of GI-active and in GI greatly influence TFTs characteristic and stability. So we optimized device characteristic on PI glass by reducing the hydrogen content in GI. Two deposition conditions were fabricated, sample C of stacked GI was deposited with 2steps of low power and high power, and sample D GI was deposited with 1step of medium power. As **Fig. 3** shows, their TFTs characteristics are similar, both have good uniformity on glass (ΔVth of different sites <1.5V). Then the PBTS were test, sample D of 1step GI is stable than sample C (as **Fig. 4**), and Vth shift of sample D was 0.48V .

In contrast to 1step (single layer of SiOx), 2steps deposition would form stacked layer of low-power/high-power SiOx, low power has a faster deposition speed (about 6.7Å/s) than high power (about 4.5Å/s). Under high speed hydrogen is difficult to escape from SiOx during deposition witch cause high hydrogen content in GI layer. During stress test at 60℃, hydrogen in low power SiOx of higher hydrogen concentration diffused into high power SiOx slowly, leading dangling bond in low power GI, and dangling bond trapped electronics which caused Vth positive shift during PBS.

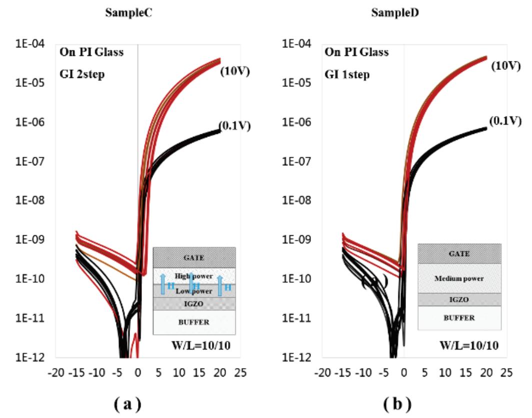

Fig. 3 The Id-Vg curve at different sites with(a)Sample C with GI 2step deposition, (b) Sample D with GI 1step deposition on PI glass.

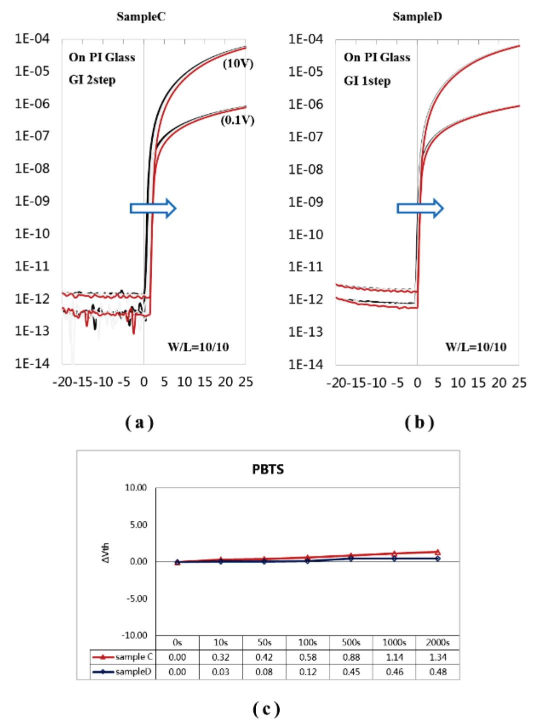

Fig. 4 The PBTS test of (a)Sample C with GI 2step deposition, (b) Sample D with GI 1step deposition on PI glass and (c) the Vth shift after PBTS.

3.3 Static bending and dynamic test

After LLO process , the static bending with a radium of 0.5mm need a long TFT test key, so we choose a TFT with a dimension of W/L=5000um/10um and measured the PBTS stability. The measure method is as **Fig. 5 (a)** and **(b)** showed, the PBTS Vth shift of static bending state was 0.97V (**Fig. 5 (c)**). And after dynamic test with a radium of 5cm for 5000cycles (**Fig. 6 (a)**), the PBTS Vth shift after 5000cycles folded was 1.00V (**Fig. 6 (c)**). The devices keep good PBTS stability and can meet the demand of curve and foldable display.

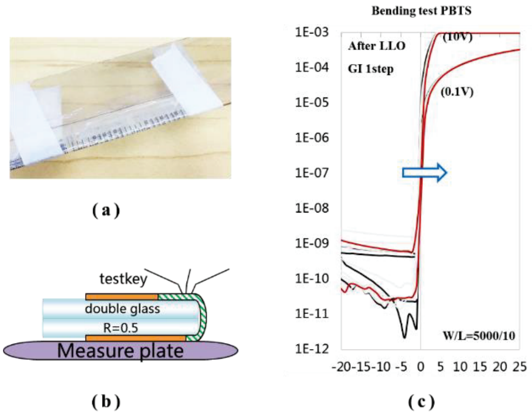

Fig. 5 (a)The picture of test key bending on glass, (b)Diagrammatic sketch of TEG measurement in bending state and(c)The PBTS test of sample D in bending state with a radium of 0.5mm

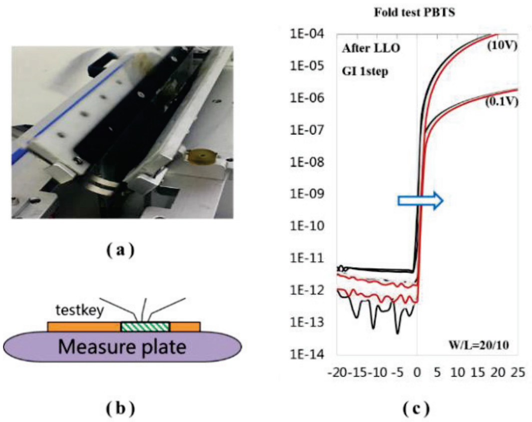

Fig. 6 (a)The folding machine, (b)Diagrammatic sketch of TEG measurement after folded and(c)The PBTS test of sample D after folded for 5000cycles with a radium of 5cm

4 Conclusion

In this paper, we have discussed the effect of PI substrate on TFTs properties , the water from polyimide thin films diffused into active layer which deteriorated device characteristic. By reducing the hydrogen content in GI could optimize device characteristic on PI glass, and 1step deposition is more stable than 2step. Finally , we did the static bending and dynamic test after LLO and TFTs on PI keep good PBTS stability.

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*These authors contributed equally to this work.

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