# **Towards Ideal Printed Organic Transistors**

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### ABSTRACT

Many organic thin-film transistors (OTFTs) exhibit nonideal current-voltage characteristics that deviate from the ideal field-effect transistor or TFTs. The physical origins include the Schottky contact injection, strong localization of carriers, interfaical dipolar disorders, and etc. To this end, we have developed theoretical understandings and various optimization method to overcome the above problems. The resulting transistors exhibit almost ideal current-voltage behaviors, featuring the high mobility values reaching 10 cm<sup>2</sup>/Vs.

## **1** INTRODUCTION

Organic-based electronic materials feature a unique combination of attractive properties, including a wide range of molecular structures to change electrical properties, tunable wavelength and intensity for absorption or emission, versatile deposition techniques and postdeposition treatments, low-temperature and low-cost processing conditions, and controllable mechanical properties. As one of the basic electronic devices, organic field-effect transistor (OFET) or thin-film transistor (OTFT) regulates conductance and provides tuning of output current in a wide range. For fundamental studies of materials, OFETs adjust carrier concentration and conductance to reveal the charge injection and transport properties of organic semiconductors. For electronic applications, OFET can act as a key logic and amplifier for large-area circuits, a driving unit for emissive display, a multifunctional unit to memorize or detect various signals.

An important issue is that the generally non-ideal characteristics appear in many OFETs and it is difficult to probe charge transport in the channel.<sup>[1]</sup> Non-ideal transistor performance has been observed for numerous devices with newly developed semiconducting nanowires, 2D nanosheets, and organic small molecules or polymers. One of the main reasons is the contact effects,<sup>[2]</sup> including work-function misalignment,[3] interfacial states.[4] semiconductor destruction,<sup>[5]</sup> anisotropic transport,<sup>[6]</sup> interfacial trapping,<sup>[7]</sup> etc. The distorted channel potential, carrier concentration, and electric fields make the operation of FETs or TFTs complicated and lead to difficulty in understanding the performance and transport properties.

Therefore, we first examine the origins of non-ideal OFETs and present our efforts in optimizing fabrications and device structures to approach ideal OFETs.

## 2 THEORIES

This section describes the discussion of non-ideal OFETs and their origins.

#### 2.1 Charge transport

The definitions of mobility for FETs are shown in Fig. 1. In the semi-classic description. In single crystals with perfect lattice and periodic potentials (Fig. 1b), electrons or holes are accelerated by the external electric field between each collision and the average time between successive collisions is defined as the mean free time. The accelerated velocity between each collision is then determined by the electric field Ex and thus the carrier mobility for single crystal is defined as  $\mu_{\text{band}} = \frac{v_{\text{d}}}{E_{\text{x}}} = \frac{q\tau}{m^*}$  $rac{q_{\Lambda}}{\sqrt{2kTm^{*}}}$  , where  $\lambda$  is the mean-free path and the subtitle band rises as the effective mass m\* characterizes the energy band. For organic crystals, values of m\* and  $\mu_{\text{band}}$  could be predicted by DFT calculations on electronic intermolecular couplina. molecular reorganization energy, molecular packing structure, and band structure with considering the electron-phonon scatterings, including all intra- and inter-molecular vibrations.<sup>[8]</sup> For polycrystals or amorphous semiconductors (Fig. 1c), various transport mechanisms have been proposed mainly by inducing localized states in band model or by directly considering the hopping process among localized states.[9]

#### 2.2 Charge injection and accumulation

Values of device mobility measured in FETs are far from the intrinsic transport properties in semiconducting channels, i.e.  $\mu_{\rm FET}$  is distinct from  $\mu_{\rm eff}.$  This is because the evaluation of n (and also  $E_X$ ) can be easily affected by the electrode-semiconductor interfaces and thus it raises the complexity in understanding, interpreting, and comparing  $\mu_{\text{FET}}$ . As the evaluated *n* may include all the mobile carriers, some part of immobile carriers, and contact-correction factors, many possible confusions have been raised with frequent discussions, especially recently. The depletion region near the interface or in the bulk would reduce the voltage gradient in the channel and thus reduce the carrier accumulation<sup>[10]</sup>. In this case, the mobility-V<sub>G</sub> dependence should be plotted together with the drain current. We summarize the typical mobility curves extracted by transfer characteristics in Fig. 2. The values are normalized to the maximum of each curve. The intrinsic mobility of disorder-free semiconductors is

almost constant (black), whereas that of disordered semiconductors generally follows the power law (grey) on account of charge hopping among localized states. When the contact resistance is small and merely affected by the gate field (i.e. resistive contact in gate tuning), the transconductance gradually decreases and leads to mobility underestimation in the linear regime (red). Such a shape can additionally be obtained if there is surface/phonon scattering, where the mobility decreases with the carrier concentration (N) as  $\mu \propto N^{-\gamma}$ , and  $\gamma$  is usually small at room temperature. If the contact resistance is significantly tuned by the gate field (i.e. gated Schottky contact), the device works in diode mode only (purple) or transits to transistor mode (blue), where the mobility change is dramatic with a sharp peak and the values can be overestimated. Therefore, the mobility needs verification with other methods. Transistors of this type also include the so-called source-gated transistor (SGT)<sup>[11]</sup> or Schottky barrier transistor (SBT)<sup>[12]</sup>. Note that the Fig. is only for illustrating the main features; the practical devices may exhibit slightly different shapes.

## 3 EXPERIMENTS AND RESULTS

This section describes our efforts in optimizing OFETs toward ideal transistors.

## 3.1 Control of coating to optimize transport

We first applied controlled spin-coating method to deposite small molecular semiconductor 2,7diocty[1]benzothieno[3,2-b]benzothiophene (C<sub>8</sub>-BTBT)<sup>[13]</sup> was selected as the semiconductor, since it has been widely investigated in printed electronics<sup>[14]</sup>. The simulation of the liquid dynamics in tiled spin-coating are shown in Fig. 3. We dissolved C8-BTBT in a mixture solvent of anisole and N, N-Dimethylformamide (DMF) (0.2 wt%). The simulated result for this mixture solvent should be similar to that on chlorobenzene, as they have similar properties. A solution droplet was placed on a SiO<sub>2</sub>/Si substrate with tunable angles of inclination from 0 to 90°. After spin-coating the ink droplet, a highly crystalline film with large single crystal domains that covered several hundred micrometers was obtained (Fig. 4a). The single crystal domains were visible under cross-polarized light, became invisible (dark) when the substrate was rotated 45°, indicating the high crystallinity and uniformity for the C8-BTBT film. High-resolution AFM was performed to characterize the regular arrangement of molecules (Fig. 4b). The crystalline thin film consists of approximately 2.7 nm molecular layers (Fig. 4c-d).

The oriented flow and crystallization that were achieved by tilted-spinning were applied to the solutionprocessed OTFT arrays. A 125-µm thick PEN film with a surface modification layer of Parylene-C was again used as a substrate. An ink of Gold nanoparticles (AuNPs) was printed on a Parylene-C surface using the surface wettability contrast that was induced by vacuum ultraviolet treatment to constitute source and drain electrodes arrays followed by the screen printing of a Cytop guide layer. The droplets self-assembled into the Cytop bank trapped in it when dropped from above even though the substrate was tilted at high degree, and stayed in the bank during spin-coating under such an acceleration. As a result, oriented crystalline thin film formed on electrodes. The domain size of a single-crystal was as large as several hundred microns to cover the channel region completely (Fig. 5a). The oriented crystals were aligned in the same direction as the transport path, which could be observed under a polarizing microscope. Next, a 900-nm Parylene-C film was deposited on it as the gate dielectric and gate electrode was printed on it, thereby composing the topgate, bottom-contact structure (Fig. 5b).

The resulting device exhibited transfer and output characteristics as shown in Fig. 5c and d. The device was turned on at a low threshold voltage of 2 V with a high on/off ratio of 107 in the saturated region. The reversed subthreshold slope, which is denoted as SS, is as low as 0.3 V/dec, and the small hysteresis between the forward and backward scanning of all curves implies the high quality of the organic semiconductor surfaces. Correspondingly, the concentration of the interface states, which is denoted as  $N_{\rm t}$ , was  $4.8 \times 10^{10}$  cm<sup>-2</sup>eV<sup>-1</sup>, which was calculated as  $N_t = \left[\frac{q \cdot SS \cdot \lg(e)}{kT} - 1\right] \frac{c_i}{q^2}$ <sup>[15]</sup>. In this equation, k, T and q are the Boltzmann constant, absolute temperature, and electron charge, respectively. The device exhibited a high  $\mu_{sat}$  value of 9.0 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>, which was the saturated mobility value that was obtained by fitting the slope of  $\sqrt{I_{
m D}}$  as a function of V<sub>G</sub>. To prevent the overestimation of carrier mobility<sup>[10]</sup>, we calculate the reliability factor<sup>[16]</sup> to assess the accuracy: the value is 90.5 %, which is close to the 100 % reliability factor of the ideal thin-film transistors.

#### 3.2 Control of contacts to optimize injection

We deposited doping layers at the interfaces of Au electrodes and organic semiconductors. The formation of charge injection layers of transition metal oxides (TMOs), such as molybdenum oxide (MoO<sub>3</sub>), vanadium oxide (V<sub>2</sub>O<sub>5</sub>) and tungsten oxide (WO<sub>3</sub>) contributed to decreasing the charge injection barrier at the contact interface. The transistor electrodes doped by TMOs can markedly increase  $\mu_{\text{FET}}$  and lower the threshold voltage. It was also reported that aqueous TMO solutions could be used for the doping process in solution-processed devices. The doped device exhibited higher µFET of 13.1 cm<sup>2</sup> V<sup>-1</sup> s<sup>-1</sup>, a smaller threshold voltage of 2.5 V, and a decreased contact resistance as compared with those in the undoped ones. Also, we prepared transistor arrays doped by V<sub>2</sub>O<sub>5</sub> or WO<sub>3</sub>, performed the characterization of charge carrier transport properties, and found that the average µFET values were obviously increased after being doped, comparing with those of undoped ones.

## 4 CONCLUSIONS

To encounter the problem of disordered charge injection and insufficient charge injection, we have developed theoretical understandings and various optimization method to approach ideal OFETs.

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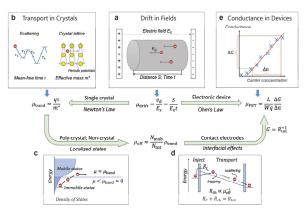


Fig. 1. The mobility path for FETs.<sup>[17]</sup> Copyright 2019, Wiley

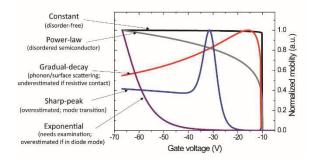


Fig. 2 Mobility curves of non-ideal FETs.<sup>[18]</sup> Copyright 2017, APS

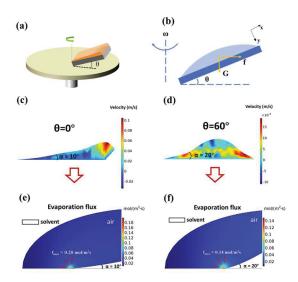


Fig. 3 Simulation of tiled spin-coating.<sup>[19]</sup> Copyright 2019, ACS

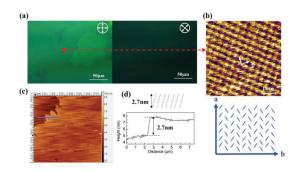


Fig. 4 Films obtained by tiled spin-coating.<sup>[19]</sup> Copyright 2019, ACS

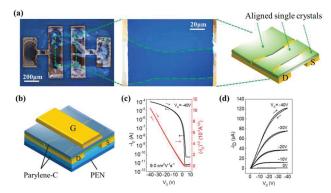


Fig. 5 Devices of OFETs after optimizing contacts.<sup>[19]</sup> Copyright 2019, ACS