Low-Temperature, Solution-Processed Inorganic p-Channel Cu-based Thin-Film Transistors and Circuits

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ABSTRACT

Developing p-type transparent semiconductors has attracted great interest over the past decades to realize complementary p-n junction devices and circuits by cost effective graphic art processes. Here we report two kinds of transparent p-type Cu-based transistors (CuI and Cu_xO), which can be synthesized using solution process at plastic-compatible temperatures.

1 INTRODUCTION

Solution-processed p-type oxide semiconductors have recently attracted increasing interests for the applications in low-cost optoelectronic devices and circuits.[1] To date, only a few compounds, e.g., SnO, Cu_xO, and NiO_x, have been demonstrated and incorporated into transistors as the p-type channels. Among these, Cu_xO is a promising candidate for p-type semiconductors due to its high Hall mobility, suitable optical properties, nontoxicity, and low costs. In initial studies, the deposition of Cu_xO semiconducting layers relied on vacuum-based deposition techniques. Recently, alternative solution-based film deposition approaches, including spin/spray coating and inkjet printing, have been actively studied due to their simplicity, low cost, air processability, and scalability for large-area fabrication. Unfortunately, most of these studies employed high annealing temperatures (≥400 °C) or complex multi-step fabrication procedures, which typically lead to low repeatability and large lab-to-lab fluctuations in device performance. In the first part, a simple solution-phase polyol reduction method was used to fabricate Cu_xO films as the active layer of transparent p-channel TFTs. The optimized Cu_xO TFTs derived from propylene glycol at 220 °C exhibited stable operation with an average filed-effect hole mobility (μ_{FE}) of 0.15 $cm^2 V^{-1} s^{-1}$ and on/off current ratio (I_{on}/I_{off}) of ~10^4. The dry air and operational stability tests also showed reliable electrical characteristics.[2]

Recent theoretical studies have shown that anions with smaller electronegativity and larger p-orbitals than O^{2-} are more effective at realizing delocalized VBM than oxides. One promising inorganic p-type candidate is copper(I) iodide (CuI), which has high conductivity (238 S cm^{-1}) as well as large E_g = 3.1 eV. The naturally abundant and environment friendly constitutional elements of CuI make it more appropriate for large scale printed transparent electronics. More importantly, CuI has much higher hole mobility (43.9 $cm^2 V^{-1} s^{-1}$ in bulk material compared with CuSCN and other p-type oxide semiconductors due to fairly small effective hole mass. In the second part, we report solution-processed p-type CuI TFTs processed at room temperature by controlling precursor concentration and CuI thickness. The optimized CuI TFTs with SiO_2 dielectric exhibited high hole mobility μ_{FE} = 0.44 $cm^2 V^{-1} s^{-1}$ with $I_{on}/I_{off} \approx 5\times10^2$. Combining a high permittivity ZrO_2 dielectric layer increases μ_{FE} to 1.93 $cm^2 V^{-1} s^{-1}$ with very low operating voltage (< 5 V). We demonstrate a complementary inverter with solution processed p-type CuI TFTs and n-type indium gallium zinc oxide (IGZO) TFTs.[3]

2 EXPERIMENT

Cu_xO solution (0.1 M) was prepared in deionized water and propylene glycol mixtures (1:5 vol/vol). The precursor solution was spin-coated on SiO_2/p^+-Si substrates at 7000 rpm for 30 s. The gel films were first baked at 150 °C for 30 min and subsequently annealed at different temperatures in air for 30 min (ambient humidity < 20 %).

CuI precursor solutions were prepared by dissolving CuI powder into acetonitrile at concentrations 3, 5, 7, 10, and 25 mg ml^{-1}. Precursor solution was filtered through a 0.2 μm syringe filter and then spun on SiO_2/Si substrates at 5000 rpm for 30 s in air. The 40-nm Au source and drain electrodes were deposited by thermal evaporation using a shadow mask.

3 RESULTS and DISCUSSION

3.1. Solution-processed Cu_xO TFTs

To investigate the electrical properties of the prepared Cu_xO thin films as channel layers in TFTs, bottom-gate top-contact (BG-TC) devices were fabricated on SiO_2/p^+-Si substrates and representative transfer curves are shown in Fig. 1a. 150 °C baking process enabled the formation of metallic Cu-dominated components. Gradually increasing the annealing temperature resulted in the phase transformation: Cu + Cu_2O + CuO→ Cu_2O + CuO → CuO. The 150 °C-baked TFTs showed insulating behavior while typical p-channel characteristic were observed and enhanced upon increasing the temperature to 220 °C. The improved hole transport was

attributed to the decomposition of residual compounds and thermally-driven grain size augmentation. The latter is expected to reduce the number of grain boundaries, associated scattering, and possible deep traps. The optimized PG-derived devices were achieved at 220 °C with an improved μ_{FE} of 0.15±0.02 $cm^2\ V^{-1}\ s^{-1}$, I_{on}/I_{off} of ~10^4, and bias-stress stability, showing excellent reproducibility (Fig. 1b).

We further investigated their hole transport properties by analyzing temperature-dependent characteristics (Fig. 1c). The device mobility decreases linearly at lower temperatures, indicating that hole transport is thermally activated. This conduction mechanism likely occurred via defects and traps within grain boundaries or between the Cu_xO/SiO_2 interface. The corresponding activation energy (E_a), *i.e.*, the energy difference between the Fermi level and VB edge, was calculated to be 0.16 eV by fitting the plots using the equation, $\mu_{FE} = \mu_0 \exp(-E_a/k_BT)$, where k_B is the Boltzmann constant. The E_a was lower than the devices prepared using sputtering ($E_a \approx 0.4$ eV), which confirmed the superiority of PG-derived polyol reduction method for the fabrication of Cu_xO TFTs. A key motivation for developing high-performance p-type oxide TFTs is to implement transparent CMOS circuits via integration with n-type oxide TFTs. The transparent CMOS inverters were then constructed by assembling Cu_xO and n-type InGaZnO TFTs. The inverter exhibited a sharp and clear signal inversion between the high and low states with negligible hysteresis (Fig. 1d). The voltage gain (dV_{out}/dV_{in}) reaches 37 at supply voltage (V_{DD}) = 60 V. To the best of our knowledge, this gain value is the highest reported to date for a solution-processed oxide TFT-based CMOS inverter.

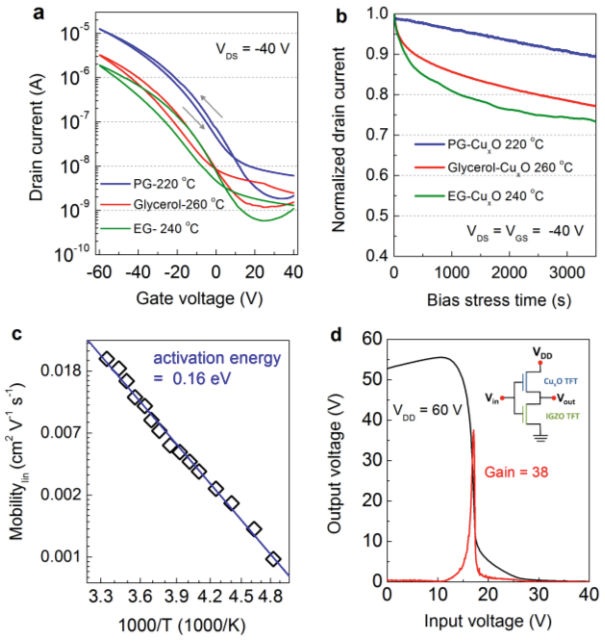

Fig. 1 (a) Transfer characteristics of the optimized Cu_xO TFTs fabricated using different polyols at the indicated temperature. (b) Negative bias stress results of the optimized Cu_xO TFTs derived from different polyols. (c) Mobility variation for the PG Cu_xO-220 TFTs measured at different temperatures. (d) Voltage transfer characteristics and gain voltage of the CMOS inverter.

3.2. RT Solution-processed CuI TFTs

Figure 2a shows transfer curves for TFTs processed from different precursor concentrations (i.e., 7, 5, and 3 mg ml^{-1}). When the CuI channel thickness reduces to ~8 nm, apparent field effect modulation of channel currents (I_{DS}) under V_{GS} was observed with $I_{on}/I_{off} > 10^2$. TFTs with 5 nm CuI channel layers exhibited the best electrical performance with average μ_{FE} = 0.42 $cm^2\ V^{-1}\ s^{-1}$, $I_{on}/I_{off} \approx 5\times10^2$, V_{TH} = 35 V, and excellent reproducibility. Importantly, these promising electrical parameters were obtained at room temperature (RT) without requiring post-treatment processing. For solution processed p-type oxides, such as Cu_xO and NiO, relatively high annealing temperatures (≥ 250°C) are required to decompose residual impurities and achieve crystalline texture, which limits their applications on plastic substrates for flexible devices. For CuI, successful achievement of solution processed CuI TFTs at RT is very beneficial from the crystallization tendency of CuI and highly volatile acetonitrile solvent, leading to negligible impurity residues in the as-coated CuI channel layer.

To emphasize the developed CuI semiconductor superiority, we demonstrated a CMOS inverter by assembling p-type CuI and n-type InGaZnO TFTs. Figure 2b shows the voltage transfer characteristics of the complementary inverter at different V_{DD}. The CMOS inverter exhibited complete rail-to-rail voltage inversion between high and low states with voltage gain >4, which would be sufficient to drive next-stage components in a logic circuit. For the further performance improvement of RT CuI TFTs, we employed oxide dielectric with high permittivity (high κ). We selected a promising high κ candidate, ZrO_2, with κ = 25 and large *bandgap* ≈ 5.8 eV.[4] Gel films containing Zr were spin-coated onto heavily doped Si substrates, followed by UV irradiation under ambient conditions. UV induced photolysis and oxidation formed dense ZrO_2 thin films at RT. The first truly RT and solution processed TFTs with Au/CuI/ZrO_2/Si structure were fabricated and output and transfer plots are shown in Fig.2c and 2d. Benefiting from the large gate capacitance of ZrO_2 dielectric, the as-prepared transistors can be operated as low as 5 V, which is quite essential for applications in mobile and low power consumption devices. CuI/ZrO_2 TFT μ_{FE} = 1.93 $cm^2\ V^{-1}\ s^{-1}$. In addition, replacing SiO_2 with ZrO_2 caused negative threshold voltage (V_{TH}) shift from 35 to -0.45 V,

indicating that device operation mode changed from depletion to enhancement. For logic circuit applications, enhancement mode transistors are preferable to depletion mode because no V_{GS} is required to switch the devices off, hence circuit design is simpler and lower power consumption. The negative V_{TH} shift implies that the ZrO_2 layer contains positive fixed charges, which can achieve negative threshold or turn-on voltage for p-channel TFTs.

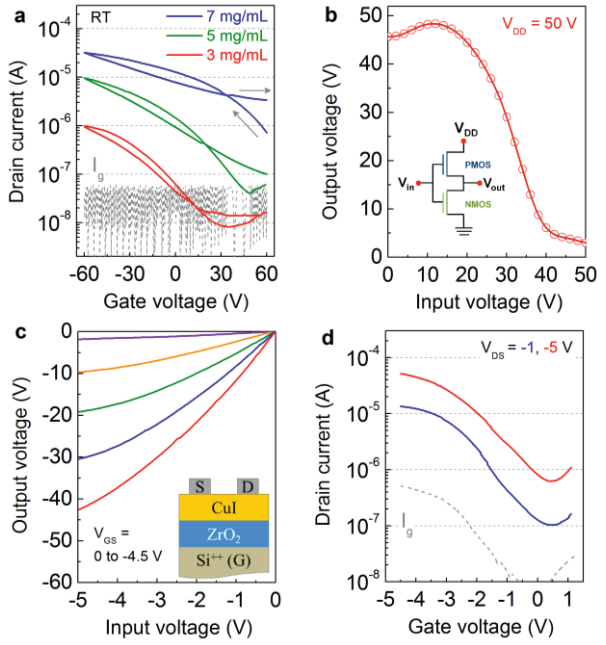

Fig. 2 (a) Transfer characteristics for the RT-deposited CuI TFTs as a function of channel thickness. (b) Voltage transfer characteristics of complementary inverter based on p-type CuI and n-type InGaZnO TFTs (c, d) Output and transfer curves of solution-processed CuI/ZrO_2 TFTs.

4 CONCLUSIONS

Herein, two kinds of solution-processed inorganic p-type Cu-based TFTs were reported. Firstly, the fabrication of low-temperature solution-processed Cu_xO TFTs using eco-friendly polyol reduction method was reported. The selection of appropriate polyalcohol, optimal channel thickness, and annealing temperature were critical for achieving good transistor performance with high operational stability. The optimized Cu_xO TFTs derived from propylene glycol at 220 °C exhibited stable operation with an average μ_{FE} of 0.15 $cm^2 V^{-1} s^{-1}$, I_{on}/I_{off} of ~10^4, and excellent reproducibility. This work aims to provide a comprehensive investigation on the electrical properties of solution-deposited Cu_xO TFTs. The optimized polyol reduction method proposed here is simple and reliable, enabling device fabrication at plastic-compatible temperatures.

In the second part, we successfully demonstrated RT solution processed p-type CuI TFTs with electrical performances strongly related to channel thickness and annealing conditions. Optimizing the precursor formulation, and CuI and gate dielectric thicknesses, produced p-type CuI/ZrO_2 TFTs with a μ_{FE} = 1.93 $cm^2 V^{-1} s^{-1}$ at low operating voltage = 5 V. We believe that this work opens the floodgate for room temperature, low cost, high performance inorganic p-type transistors for diverse opto/electronic devices.

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