Capacitance-Voltage Characteristics of Solution-Based HfZr-Silicate Gate Dielectrics

Nara Lee, Pyungho Choi, and Byoungdeog Choi

Department of Electrical and Computer Engineering, Sungkyunkwan University, 2066 Seoubu-ro, Jangan-gu, Suwon-si, Gyeonggi-do 16419, Republic of Korea

Keywords: HfZr-Silicate, High-k dielectrics, MOS, Solution process

ABSTRACT

In this study, Al/$(HfZrO_4)_{1-x}(SiO_2)_x$/p-Si capacitors were fabricated and evaluated as a function of SiO_2 content in the films. From the result, electrical properties enhanced such as oxide charge and breakdown voltage as the SiO_2 concentration x increased and reliability improved as well.

1 INTRODUCTION

High-k dielectrics have been considered as an alternate for reducing driving voltage and scale of device in thin-film-transistors [1, 2]. Among these materials, HfO_2- and ZrO_2-based dielectrics have been recommended as the gate insulators in TFTs because of their high dielectric constant (κ), large band-gap energy, and excellent interfacial properties with silicon substrate [3]. However, oxide materials have stability issues resulting from the oxide charges [4]. In this report, we introduce solution-based $(HfZrO_4)_{1-x}(SiO_2)_x$ (HfZr-silicate) films and discuss their trap-related oxide properties evaluated using the capacitance-voltage (C-V), and current-voltage (J-V) characterization method.

2 EXPERIMENT

P-type silicon wafers (resistivity of 1-30 Ω·cm), used as a substrate, were prepared by RCA cleaning. 0.2M HfZr-Silicate solution ($(HfZrO_4)_{1-x}(SiO_2)_x$) was fabricated dissolving Hafnium dichloride oxide octahydrate ($HfCl_2O{\cdot}8H_2O$), Zirconium (IV) oxychloride octahydrate ($Cl_2OZr{\cdot}8H_2O$) and Tetraethyl orthosilicate ($C_9H_{20}O_4Si$) into 2-Methoxyethanol (2-MOE). The molar composition ratio of solution was varied by increasing silicate (x=0, 0.1, 0.2, 0.3, 0.4, 0.5). The solution was stirred at 1000 rpm at room temperature (RT) for 3 hours. The HfZr-Silicate solution was filtered through a 0.2 μm disposable membrane filter and spin coated at 3000 rpm for 30s on a silicon wafer. Spin coated HfZr-Silicate films were pre-annealed at 200 °C for 10 min and 5 min cooling at RT. This cycle was repeated five times and thickness was 90nm measured from Spectroscopic ellipsometry (SE). Annealing was done at 400 °C and 600 °C for 10 min in rapid thermal annealing (RTA). 70 nm thick Al electrode was deposited by e-beam evaporator. The capacitance-voltage (C-V) characteristics were obtained from Agilent E4980A precision LCR meter at 100 kHz frequency. The current-voltage (J-V) characteristics were measured by the Agilent B1500A.

3 RESULTS and DISCUSSION

Figure 1 (a) shows capacitance versus voltage curves of Al/ $(HfZrO_4)_{1-x}(SiO_2)_x$/ p-Si structure as function of SiO_2 content x. As we expected, oxide capacitance (C_{ox}) decreased from 97.93 pF to 47.03 pF as content of SiO_2 increased up to 50 %. Dielectric constant (SiO_2, HfO_2, and ZrO_2 are 3.9, 25, and 25 for each) decreased from 14.08 to 6.76. Also, we can observe C-V curves shifted toward negative gate bias direction and flat band voltage shifted from 3.79V to -2.39V which can confirm in Table. 1. HfO_2 and ZrO_2 annealed above 400 °C have significant amount of negative fixed oxide charges, and SiO_2 reduces negatively charged oxide defects [5]. Furthermore, doping of SiO_2 successfully improves interface between gate dielectric and substrate. As shown in Figure 1 (b), interface trap density decreases from 5.27×10^{11} $cm^{-2}eV^{-1}$ to 1.16×10^{11} $cm^{-2}eV^{-1}$ and these were extracted by terman method. Silicate-Si has similar bond with SiO_2-Si, which means silicate plays a role of passivation of the gate dielectric and substrate interface [6]. Border trap (N_{bt}) was also extracted from the hysterical C-V characteristics and decreased from 1.92×10^{12} cm^{-2} to 5.42×10^{10} cm^{-2} (as shown in Table. 1). This also can confirm that SiO_2 incorporation enhanced interface between gate dielectric and substrate. Furthermore, high temperature annealing makes layer thinner so that devices annealed at 600 ºC have higher C_{ox} compared with 400 ºC as shown in Figure 2. And rest of C-V properties have same tendency with devices annealed at 400 ºC

As content of silicate increases bandgap also rises, and in this reason, leakage current significantly decreases from 3.76×10^{-8} A/cm to 3.71×10^{-10} A/cm [7]. We can also observe breakdown voltage increases from Figure 1 (c) and Figure 3 (a). HfZr-Silicate gate dielectric shows high breakdown voltage (V_{BD}) compare with $HfSiO_x$, HfO_2, and ZrO_2 [8]. This indicates

incorporation of SiO_2 improves durability of gate dielectric. HfZr-Silicate annealed at 600 ºC shows same J-V tendency with 400 ºC, which can confirm in Figure 3. Breakdown voltage decreases as SiO_2 content increases at both condition, however, 600 ºC annealed devices show lower breakdown voltage than 400 ºC. HfO_2, ZrO_2, and SiO_2 are amorphous phase at 400 ºC, on the other hand, after 600 ºC annealing, HfO_2 and ZrO_2 shows multiphase and so does $HfSiO_x$ [9]. Tetragonal phase HfO_2 and ZrO_2 lowering breakdown voltage because of weaken the polar molecular bonds [10]. Leakage current at -1 V is also compared in Figure 3 (b), and 600 ºC annealed devices have higher leakage current than 400 ºC. Consequently, higher leakage current of 600 ºC annealed HfZr-Silicate can be explained by polycrystalline phase, and its grain boundaries and grain act as current path.

4 CONCLUSIONS

We confirmed that incorporation of SiO_2 into the $HfZrO_4$ films annealed 400 ºC, and 600 ºC both enhanced the electrical properties of the devices. By improving the dielectric quality not only reduce of oxide charge but also leakage current and breakdown voltage. Annealed at 600 ºC have high capacitance so that apply to high performance TFTs can be successful. However, it also shows instability such as degradation of breakdown voltage compared to 400 ºC. On the other hand, 400 ºC annealed HfZr-Silicate dielectric has high dielectric constant, low defects, low leakage current, and high breakdown voltage. In this reason, 400 ºC annealed HfZr-Silicate dielectric is attractive candidate for TFT and also flexible devices due to its low process temperature.

REFERENCES

[1] Si Joon Kim, Seokhyun Yoon, and Hyun Jae Kim, "Review of solution-processed oxide thin-film transistors," Japanese Journal of Applied Physics, Vol. 53, pp. 02BA02 (2014).

[2] Christophe Avis, Youn Goo Kim and Jin Jang, "Solution processed hafnium oxide as a gate insulator for low-voltage oxide thin-film transistors," Journal of Materials Chemistry, Vil. 22, pp. 17415 (2012).

[3] Noriyuki Miyata, "Study of Direct-Contact HfO_2/Si Interfaces," Materials, Vol. 5, pp. 512-527 (2012).

[4] Yana Gao, Jianhua Zhang, and Xifeng Li, "Solution-Processed Zirconium Oxide Gate Insulators for Top Gate and Low Operating voltage Thin-Film Transistor," Display Technology, Vol. 11, pp. 764-767 (2015).

[5] Rajbir Singh, Vandana, Jagannath Panigrahi and P. K. Singh, "Plasma assisted atomic layer deposited hafnium oxide films for silicon surface passivation," RSC Adv, Vol. 9, pp. 97720-97727 (2016).

[6] S. Monaghan, J. C. Greer, and S. D. Elliott, "Atomic scale model interfaces between high-k hafnium silicates and silicon," PHYSICAL REVIEW B, Vol. 75, pp. 245304 (2007).

[7] S. Hall, O. Buiu, I. Z. Mitrovic, Y. Lu, W. M. Davey, "High-k dielectric stacks for nanisclaed SOI devices," Chemistry and Materials Science, pp. 3-18 (2007).

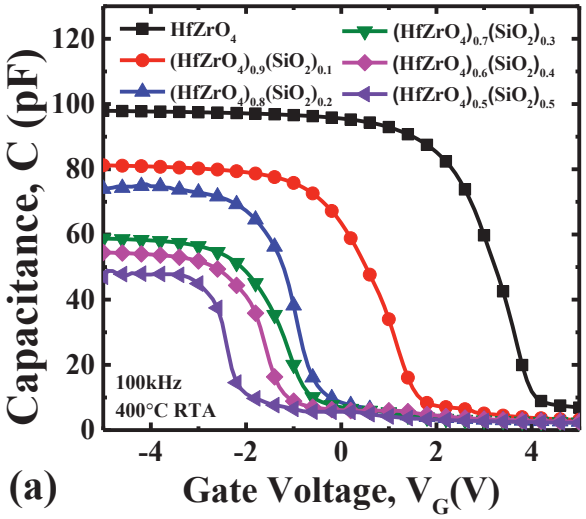
[8] Y. N. Gao, Y. L. Xu, J. G. Lu, J. H. Zhang and X. F. Li, "solution processable amorphous hafnium silicate dielectrics and their application in oxide thin film transistors." Journal of Materials Chemistry C, Vol. 3, pp. 11497 (2015).

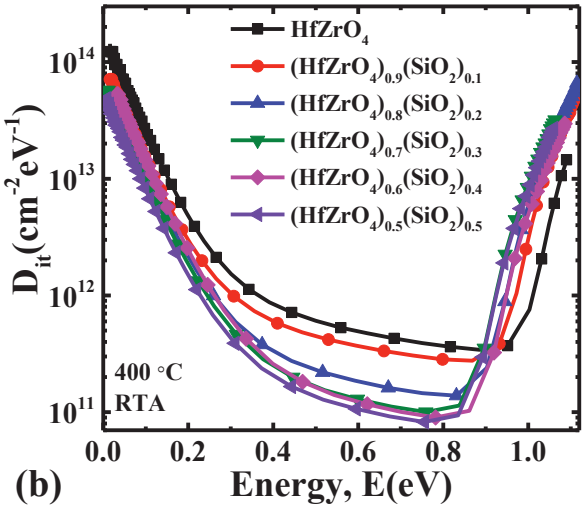
[9] Andrzej Taube, Robert Mroczynski, Katarzyna Korwin-Mikke, Sylwia Gieraltowska, Jan Szmidt, and Anna Piotroska, "Effect of the post-degradation annealing on electrical characteristics of MIS structures with HfO_2/SiO_2 gate dielectric stacks," Materials Science and Engineering: B, Vol. 177, pp. 1281-1285 (2012).

[10] J. McPherson, J-Y. Kim, A. Shanware, and H. Mogul, "Thermochemical description of dielectric breakdown in high dielectric constant materials," APPLIED PHYSICS LETTERS, Vol. 82, pp. 2121 (2003).

Table. 1 Electrical properties of $(HfZrO_4)_{1-x}(SiO_2)_x$ annealed at 400 ºC

Content x	N_{bt} (cm^{-2})	V_{FB} (V)
$HfZrO_4$	1.92×10^{12}	3.79
0.1	9.25×10^{11}	1.28
0.2	4.54×10^{11}	-0.76
0.3	1.59×10^{11}	-1.07
0.4	1.00×10^{11}	-1.61
0.5	5.42×10^{10}	-2.39





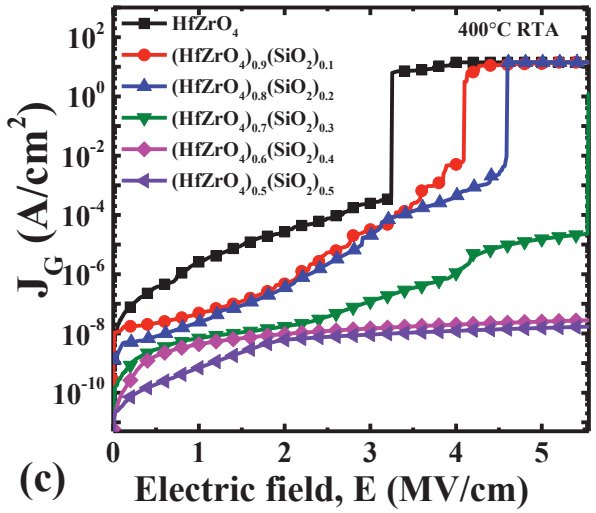


Fig. 1 (a) C-V, (b) Interface trap density and (c) J-V curves for $(HfZrO_4)_{1-x}(SiO_2)_x$ annealed at 400 ºC (x=0, 0.1, 0.2, 0.3, 0.4, 0.5)

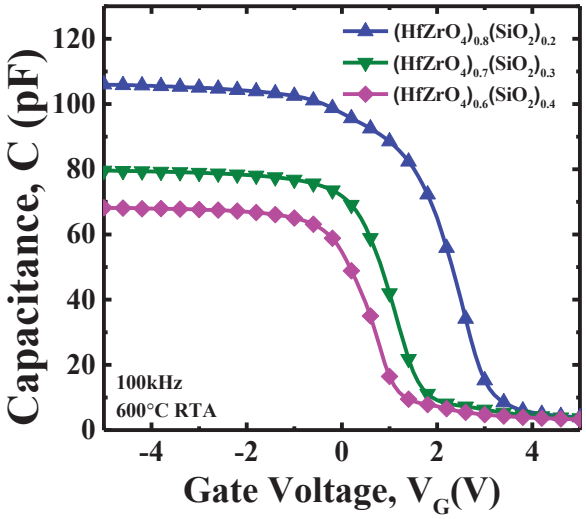
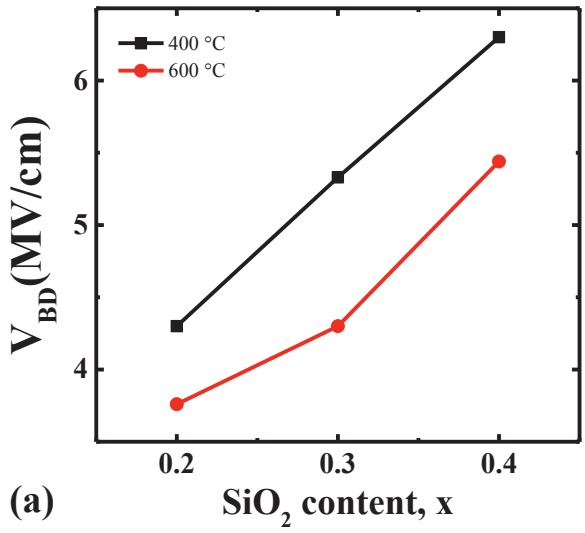


Fig. 2 C-V curve for $(HfZrO_4)_{1-x}(SiO_2)_x$ annealed at 600 ºC (x=0.2, 0.3, 0.4)



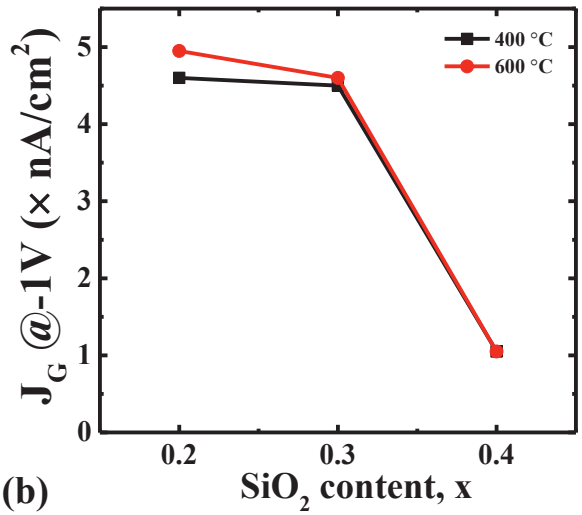


Fig. 3 (a) Breakdown voltage and (b) Leakage current density annealed at 400 ºC, 600 ºC ($(HfZrO_4)_{1-x}(SiO_2)_x$)