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High Performance TFTs with IGZO and LTPS Hybrid Structure for AMOLED Display.

Shogo Murashige, Mehadi Aman, Yujiro Takeda, Izumi Ishida, Masahito Sano, Kaoru Yamamoto, Kazuatsu Ito, Kohei Tanaka and Hiroshi Matsukizono

murashige.shogo@sharp.co.jp
Sharp Display Technology Corporation
2613-1, Ichinomoto-cho, Tenri, Nara 632-8567, Japan
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ABSTRACT

We have developed an AMOLED panel using hybrid backplane technology with IGZO and LTPS. This panel contains both Gate-on-Array (GOA) circuits and pixel circuit with high reliability IGZO and LTPS TFTs. The hybrid backplane AMOLED panel can operate between 1 and 120 Hz, which enables both high refresh rate and low standby power display applications. We operated the AMOLED panel at 60°C for 1,000 hours and it remain operational without any display problem.

1 INTRODUCTION

Recent mobile display is required to operate at low frequencies because of its low power consumption due to the limited amount of battery. High refresh rate driving is also needed to serve various purpose like gamming, writing etc. Some reports have summarized about hybrid pixel circuit of LTPS and oxide TFT (IGZO) to overcome this problem [1]. In our previous work, we reported our hybrid technology [2]. Figure 1 (a) shows our proposed pixel circuit. In order to adapt low refresh rate driving, it is necessary to keep T4 gate potential given level during long pause period. Therefore, T1 and T2 connected to T4 gate node should be IGZO. Two types of control signals are needed to drive this pixel circuit. pScan is to drive p-LTPS TFTs and nScan is to drive IGZO TFTs. Figure 1 (b) shows the proposed GOA which can generate both pScan signal and nScan signal simultaneously.

In this article, we describe the fabrication method of hybrid backplane for AMOLED display with CMOS operation of both IGZO and LTPS TFTs. To realize CMOS operation in the GOA, high reliable n-type IGZO and p-type LTPS has been fabricated. There has been few research about hybrid GOA; however, only a few of them have been implemented in the display manufacture because of the complexity of LTPS and IGZO hybrid process. We developed a fabrication method to enhance the uniformity and reliability of both IGZO TFTs in GOA and pixel circuit. For mass production, one of the criteria is display lifetime under various aging condition. We also explain the impact of the IGZO TFTs performance on the hybrid-AMOLED panel lifetime. Finally, the specification and the power consumption of the display will be explained.

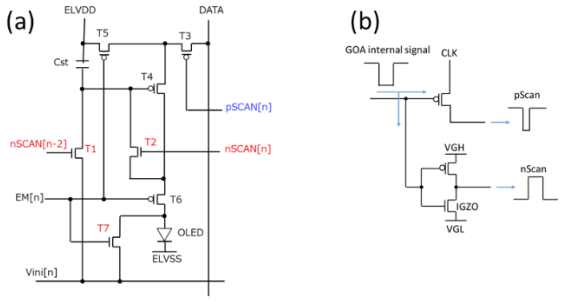

Fig. 1 (a) Pixel circuit with IGZO and p-LTPS TFTs, (b) CMOS operation image of GOA circuit.

2 EXPERIMENT

2.1 TFT structure

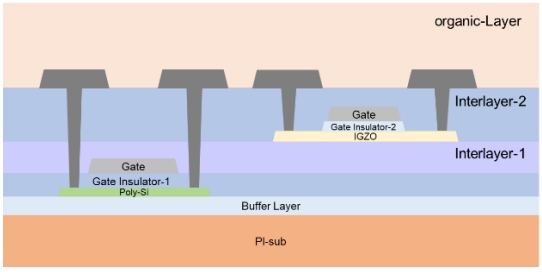

Fig. 2 Fabricated hybrid LTPS and IGZO TFTs.

Hybrid TFT structure with LTPS and IGZO are shown in Figure 2. Buffer layer is deposited on the Polyimide (PI) substrate, followed by p-type LTPS TFT. Silicon (Si) layer is crystallized by using laser annealing. After forming an interlayer film, which is optimized for both LTPS and oxide semiconductor, a top gate IGZO TFT was fabricated. The source and drain electrodes, and the contact holes of the LTPS and IGZO TFTs were formed simultaneously. The top gate insulator (TGI-2) of the IGZO was formed by the plasma enhanced chemical vapor deposition (PE-CVD) method and optimized to improve IGZO TFTs electrical properties and the reliability. An organic layer was deposited in between the hybrid backplane and the OLED layers. Details of the OLED fabrication have been explained elsewhere [3].

3 RESULTS AND DISCUSSION

3.1 Short channel IGZO TFT

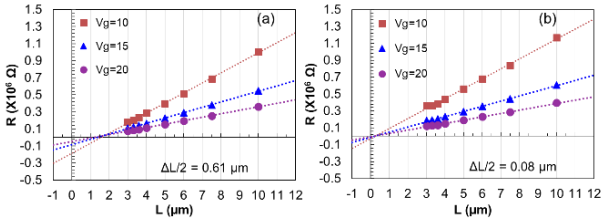

Fig. 3 Channel length for various V_g (a) before and (b) after process optimization.

High resolution display requires small ΔL region to reduce pixel size. For the IGZO-TFTs, the edge of the intrinsic channel layer can be reduced due to the source/drain n+ doping process. When the effective channel length (L_{eff} = L-ΔL) reduce the threshold voltage (V_{th}) trend to negative and worse the panel reliability. Figure 3 shows total resistance as a function of the channel length. Intrinsic channel lengths were varied from 3 μm to 10 μm. The applied gate voltage (V_{gs}) was varied from 10 V to 20 V at a drain voltage (V_{ds}) of 0.1 V. The distance from the edge of the channel (ΔL/2) of the reference process shown in Fig. 3 (a) is 0.61 μm. After optimized the source/drain n+ doping process the ΔL/2 value improved to 0.23 μm. For further improvement, we have optimized the interlayer-2 (ILD-2) as shown in Fig 2. We have introduced a low hydrogen (H) contained plasma-enhanced chemical vapor deposited (PE-CVD) dielectric layer as ILD-2. After optimized both the source/drain n+ doping process and ILD-2 as shown in Fig. 3 (b), we have achieved a ΔL/2 of 0.08 μm. By the optimized process, channel length shortening is almost negligible, thus, we were able to fabricate uniform IGZO TFTs for the hybrid pixel and GOA.

3.2 TFT performance and uniformity

Figure 4 (a) shows the V_{th} of the IGZO pixel TFTs, with a channel width and length of 2.6 and 4.0 μm as a function of cumulative probability for the TFTs of short channel optimized process. The standard deviation (σ) of V_{th} for the TFTs with ΔL/2 of 0.61 (before optimization), 0.23, and 0.08 (after optimization) μm are 0.80, 0.41, and 0.16 V, respectively.

The I_{ds}-V_{gs} characteristics of the IGZO TFTs for GOA showed very high on current of 1.3 x 10^{-5} A and 1.5 x 10^{-3} A at V_{ds} of 0.1 and 10.0 V, respectively. The field effect mobility (μ_{FE}) was typically 7.3 cm^2/Vs at 13 points on the G4.5 PI/glass substrates. As shown in Fig. 1 (a), the current flowing through the OLED device is controlled by applying voltage to the driving LTPS transistor (T4). Therefore, not only IGZO TFTs but also high V_{th} uniformity and low leakage current of p-LTPS (T4) is needed to reduce mura in the panel. The p-LTPS TFT shows good

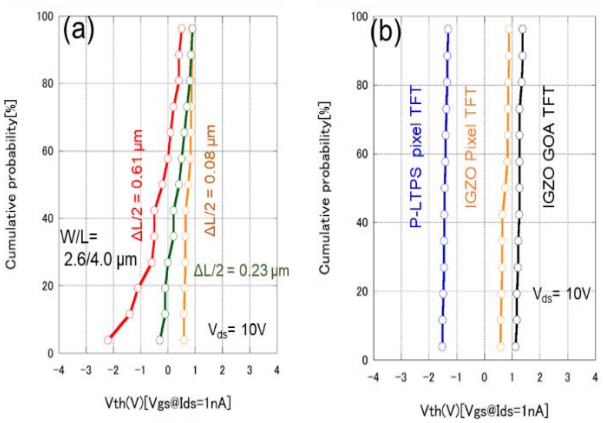

Fig. 4 (a) V_{th} uniformity of IGZO TFTs with various Δ L/2. (b) V_{th} uniformity of IGZO and LTPS TFTs.

TFT characteristics. The field effect mobility (μ_{FE}) of the p-LTPS TFT was 84.2 cm^2/Vs. It indicate that the LTPS TFTs is unaffected by the following IGZO TFT process. Figure 4 (b) shows the V_{th} as a function of cumulative probability the standard deviation (σ) of V_{th} for the P-LTPS, IGZO TFTs at GOA, and IGZO pixel are 0.14, 0.10, and 0.16 V, respectively.

3.3 Bias stress reliability of IGZO TFTs

The reliability of the IGZO TFTs were evaluated to realize the impact of IGZO TFT's performance on the AMOLED panel. The positive bias temperature stress (PBTS) measurement was conducted for the IGZO GOA TFT. On the other hand, the negative bias temperature stress (NBTS) and negative bias temperature illumination stress (NBTIS) were measured for the IGZO pixel TFTs. The gate bias stress of +20 V and -20 V for 3600 sec at 60°C was applied during PBT and NBT, respectively. Figure 5 (a) shows the V_{th} shift as a function of stress time, under PBT and NBT for the reference and optimized processed TFTs. Under PBT stress a large positive V_{th} shift (1.33 V) can be observed for the reference processed TFT. Under NBTS, after 3600 sec the V_{th} shift is 0.63 V towards negative direction. These large V_{th} shift under PBT and NBT indicate trap sites in the IGZO/TGI-2 interface. To improve the TFT reliability, the deposition condition of TGI-2 was investigated intensively. After TGI-2 deposition condition adjustment, quality of TGI-2 layer has been improved. In addition to that, plasma damage to the IGZO channel during TGI-2 deposition has been reduced. Moreover, by balancing the hydrogen diffusion from TGI-2 to TGI-2/IGZO interface, we were able to reduce the interface defect sites [4]. After optimized the TGI-2 deposition condition, V_{th} shifted +0.21 V and -0.24 V under PBT and NBT, respectively. Figure 5(b) shows the V_{th} shift (ΔV_{th}) of the IGZO pixel TFTs under negative bias temperature illumination stress (NBTIS), as a function of stress time. The NBTIS was conducted as similar condition of the

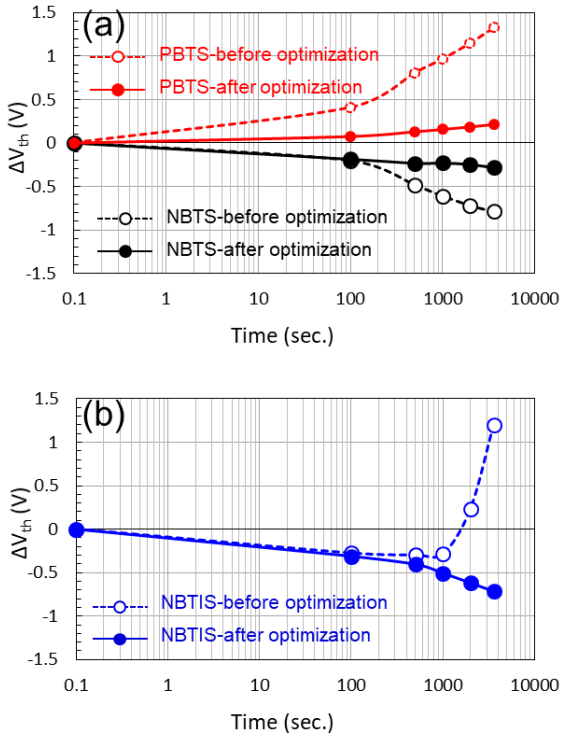

Fig. 5 (a) PBTS, NBTS and (b) NBTIS shifts of Vth.

NBT with an LED-illuminated white light of 2,000 Lux. Under NBTIS the V_{th} shifted negative until 1,000 s, however, after that time period the V_{th} start to shift positive with on current degradation and hump. It was assumed that the back-channel interface of the IGZO TFT formed by the ILD-1 might be caused electron or hole trapping during NBTIS. We have introduced an ILD-1 layer that can block hydrogen and/or hydroxyl group from underneath layers. After process optimization, V_{th} of the IGZO TFTs shift negatively with time. After 3,600 s, the V_{th} shifted -0.61 V under NBTIS. The optimized processed TFT shows excellent stability under NBTIS without on-current degradation.

3.4 Hybrid-backplane AMOLED panels reliability under aging

The aging properties of AMOLED panels are very important for the estimation of the lifetime. In general, defects in AMOLED panels accelerate with aging. Both OLEDs and TFTs are the root cause of the AMOLED panel's lifetime degradation. In a hybrid-backplane panel, both LTPS and IGZO TFTs properties affect the panels lifetime. Therefore, ensuring the reliability and uniformity of the IGZO TFT array is important for manufacturing hybrid-backplane AMOLED panels [5]. The reliability of the IGZO GOA TFT can be evaluated by measuring the AMOLED panel's voltage margin (Vpp margin) operate normally with respect to the input voltage. Figure 6 (a) shows the result of Vpp margin of reference and optimize processed hybrid-backplane panels operated at 60ºC for 1,000 h. The reference process panel may become defective during 1,000 h of driving, while the optimized process panel can be operated more than 1,000 h. These Vpp margins can be correlated with PBTS of the IGZO GOA TFT.

When IGZO TFTs in the pixel circuit shift positively, the voltage margin (on-margin) on the high side of nSCAN decreases, and conversely, when it shifts negative, the voltage margin (off-margin) on the low side of nSCAN decreases. Figures 6 (b) show the results of On-margin voltage and Off-margin voltage evaluation when the panel is driven for 1,000 h at 60ºC. If it is driven for 1,000 h before the process improvement, it is expected that malfunction will occur during use, but after the process improvement, a margin for normal driving is secured even after driving more than 1,000 h.

Moreover, we have also investigated the panel reliability under high humidity of 95% and the panels show excellent reliability both at 1 and 120 Hz operation. From the results described above, it was confirmed that the optimized processed hybrid-backplane AMOLED panel Vpp, on, and off margin is good enough for operating the panel more than 1,000 h. This is may be due to the improved IGZO pixel and GOA TFTs uniformity and reliability after process optimization.

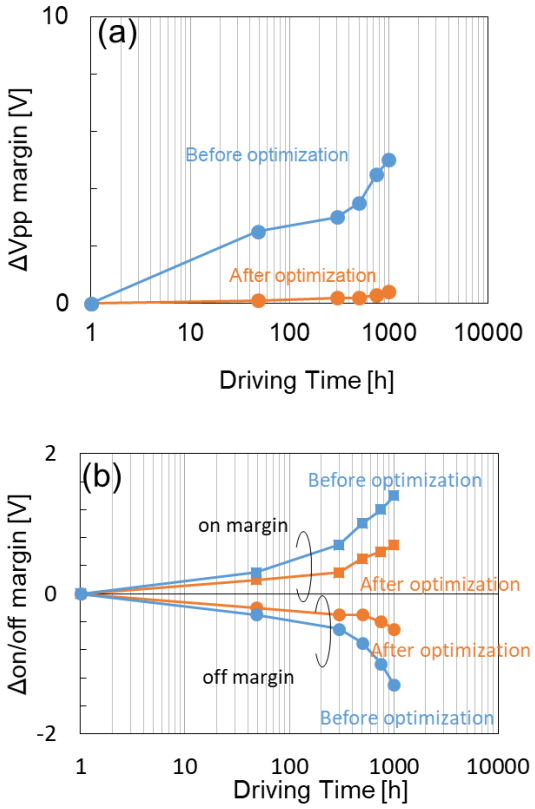

Fig. 6 AMOLED panel lifetime investigation (a) Vpp, (b) on/off margin for 1,000 h

3.5 PROTOTYPE HYBRID-AMOLED DISPLAY

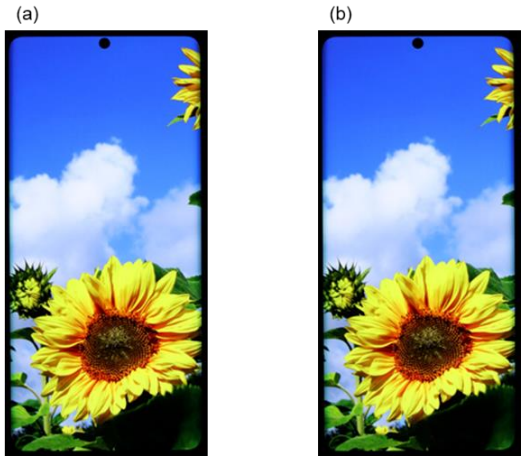

Fig. 7 Picture of the fabricated panel (a) before aging, (b) after 1,000h aging

Table 1 panel specification

Parameters	Specification
Screen Diagonal	6.58 inch
Resolution	1260 × RGBG × 2730
Pixel Pitch	55.6μm × 55.6μm
Pixel Density	457 ppi
Emission Type	Top Emission
TFT Process	Top – Gate IGZO + p-type LTPS
Frame Rate	1～120Hz

Figure 7 (a) shows the flexible AMOLED with 6.58-inch using our Top-gate IGZO and p-LTPS TFT hybrid backplane technology. The specification of the display is listed in the Table 1. The module driving test is operated with the same modular system as the general mobile phone. Figure 7 (b) shows the same AMOLED panel after 1,000 h aging at 60ºC. The panels show high reliability under high temperature and high temperature and high humidity tests.. The picture of the display shown in this paper is operating at 1 Hz, however without any bright spot or mura. Figure 8 shows the power consumption evaluated with the prototype OLED panel when displaying the picture shown in Figure 7. The power consumption can be divided into two segments, driving part (Logic + Analog) and emission part (EL). The power consumption of the driving part can be reduced at lower refresh rate. As a result, the total power consumption at 1 Hz drive including emission part can be reduced to 70% approximately compared to the 120 Hz drive. Therefore, the proposed Pixel and GOA circuit using top-gate n-oxide and p-LTPS TFT is suitable for high refresh rate and low power consumption AMOLED display.

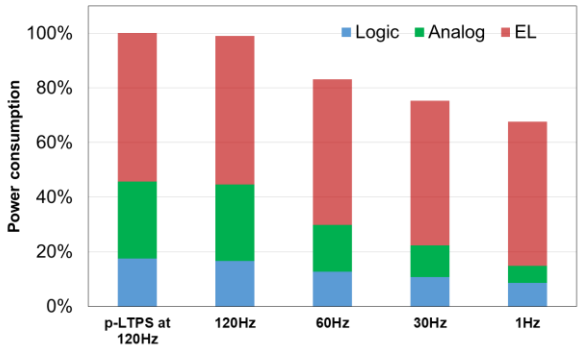

Fig. 8 Power consumption evaluation result.

4 CONCLUSIONS

An AMOLED panel using hybrid backplane technology based on p-type LTPS and n-type oxide has been successfully manufactured. The AMOLED panel lifetime has markedly enhanced by improving IGZO TFT's uniformity and reliability even in high temperature and high humidity condition. After the process improvement, panel can be drive more than 1,000 h without any display failure. Furthermore, the AMOLED can be operated at a variable refresh rate between 1 and 120 Hz. Also, the total power consumption at 1 Hz drive including emission part can be reduced to 70%.

REFERENCES

[1] T.-K. Chang, C.-W. Lin, S. Chang “LTPO TFT Technology for AMOLEDs” SID 2019 Digest, 39.3, pp. 545-548, (2019)

[2] Yonebayashi R, Tanaka K, Okada K, Yamamoto K, Yamamoto K, Uchida S, Aoki T, Takeda Y, Furukawa H, Ito K, Katoh H. “High refresh rate and low power consumption AMOLED panel using top‐gate n‐oxide and p‐LTPS TFTs” Journal of the Society for Information Display. 2020 Apr;28(4):350-9.

[3] Sonoda T, Murashige S, Tanaka K, Takase K, Katoh H, Kataoka Y, Usui T, Okada T, Shimizu T. “30-inch 4K Rollable AM-OLED Display” In2020 27th International Workshop on Active-Matrix Flatpanel Displays and Devices (AM-FPD) 2020 Sep 1 (pp. 35-38). IEEE.

[4] Y. Takeda, S. Kobayashi, S. Murashige, K. Ito,I. Ishida, S. Nakajima, H. Matsukizono, and N. Makita, "Development of high mobility top gate IGZO‐TFT for OLED display" SID Symposium Digest of Technical Papers. Vol. 50. No. 1. 516-519 (2019).

[5] M. Aman, Y.Takeda, K. Ito, K. Yamamoto, K. Tanaka, H. Matsukizono, W. Nakamura, N. Makita, “Reliability improvement of IGZO-TFT in hybrid process with LTPS” Journal of the Society for Information Display. 2021 May;29(5):416-427.