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Oxide Thin-film Transistors Driven from Substrate Backside Using Three-dimensional Wires

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ABSTRACT

This study proposes an oxide thin-film transistor (TFT) structure that enables signal input from the backside of the polyimide film substrate using three-dimensional wires that penetrate the substrate. TFTs with channel lengths down to 3 μm exhibit clear switching behavior with an on/off current ratio of over 10^7. A trench structure is also proposed to improve the yield of the proposed TFTs.

1 INTRODUCTION

Tiled displays [1][2], which comprise multiple panel units, offer customization in terms of display size, shape, and aspect ratio. Flexible panel units would allow the realization of curved tiled displays. However, the bezels of conventional panel units cannot be eliminated because signal wires are required at the periphery of a panel unit to input signals into the thin-film transistors (TFTs) in pixel circuits. As a result, tiled displays have noticeable seams between panel units. If signals can be input into the TFTs from the backside of the panel units instead of the periphery, bezel-less panel units can be realized, enabling seamless tiling.

In this work, we propose an oxide TFT structure that enables signal input from the backside of the substrate for the realization of bezel-less flexible panel units. By using three-dimensional (3D) wires that penetrate an ultrathin polyimide (PI) film substrate, we developed oxide TFTs that can be driven from the backside of the PI film substrate. We also propose a trench structure to suppress the influence of wrinkles that form on a TFT array after a laser lift-off (LLO) process. This structure effectively improves the yield of the proposed TFTs.

2 EXPERIMENTAL METHODS

Figure 1 shows a cross-sectional view of the proposed oxide TFTs with 3D wires. The TFTs were fabricated as follows. After the formation of a 50-nm-thick SiN underlayer on a 2-μm-thick PI film fixed to a glass substrate (denoted as the first glass substrate), back-channel-etched (BCE) In-Sn-Zn-O (ITZO) TFTs [3] were formed on the underlayer using a photolithography process. The channel length (L) was in the range of 2 to 10 μm and the channel width (W) was 10 μm. Note that the SiN underlayer was used to prevent delamination of the gate insulator (SiO_2) after immersion in the developing solution, as shown in Fig. 2. Next, an adhesive film and another glass substrate (denoted as the second glass substrate) were attached to the top of the PI film. The PI film with the second glass substrate was then delaminated from the first glass substrate to expose the backside of the PI film by using an LLO process. After a solution-processed planarization layer [4] was formed on the backside, contact holes that penetrated all layers, namely the planarization layer, PI film, underlayer, and gate insulator, were formed by dry etching using a CF_4/O_2 gas mixture. Mo alloy 3D wires and backside electrodes were then formed to connect the frontside and backside electrodes. Finally, the adhesive film and the second glass substrate were delaminated.

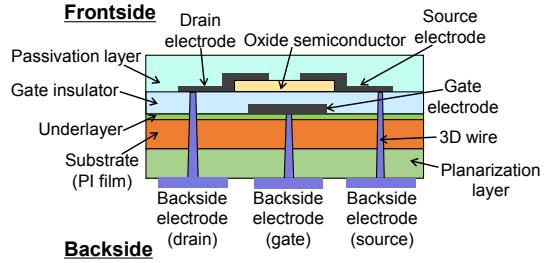

Fig. 1. Cross-sectional view of oxide TFTs driven from substrate backside using 3D wires.

3 RESULTS AND DISCUSSION

Figures 3(a) and 3(b) show optical micrographs of a fabricated BCE-ITZO-TFT (W/L=10 μm/10 μm) taken from the frontside and backside, respectively, of the PI film substrate. Multiple 3D wires were used to connect the frontside and backside electrodes, as shown in Fig. 3 (c). The diameter of the contact holes measured at the

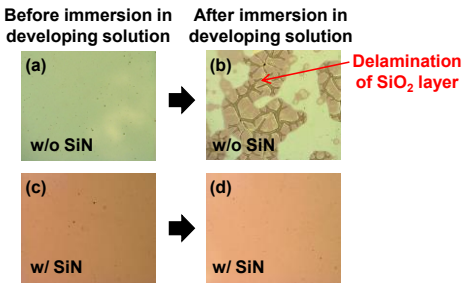

Fig. 2. Optical micrographs of PI films (a), (c) before and (b), (d) after immersion in developing solution. Note that a 200-nm-thick SiO_2 layer was sputtered onto the PI films with and without a 50-nm-thick SiN underlayer.

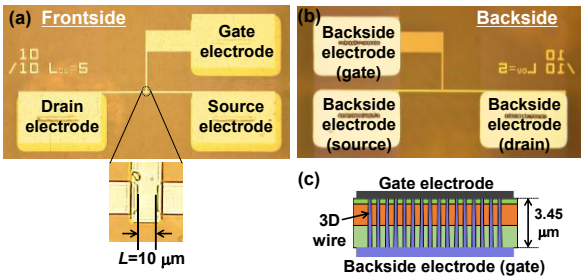

Fig. 3. Optical micrographs of a fabricated BCE-ITZO-TFT taken from the (a) frontside and (b) backside of the PI film substrate. (c) Cross-sectional view of the structure between the frontside and backside gate electrodes.

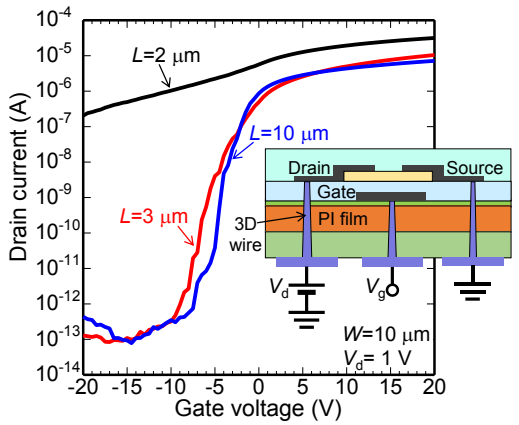

Fig. 4. Transfer characteristics of BCE-ITZO-TFTs driven from the backside of the PI film substrate using 3D wires. V_d and V_g are the drain and gate voltages, respectively.

frontside electrodes was about 20 μm. This diameter can be further reduced by optimizing the dry etching conditions.

Figure 4 shows the transfer characteristics of BCE-ITZO-TFTs driven from the backside of the PI film substrate using 3D wires. The TFTs with L from 10 μm down to 3 μm exhibited clear switching behavior with an on/off current ratio of more than 10^7. The TFT with L of 2 μm showed significantly degraded characteristics. This degradation can be attributed to damage induced by the BCE and LLO processes. Therefore, further improvement of the fabrication process is required.

Figure 5 shows the wrinkles that formed on the TFT array after the LLO process. They are attributed to strong compressive stress due to the SiO_2 layer, which was used as the gate insulator. The wrinkles appear at random locations and are oriented in random directions, as shown in Fig. 5(a). They caused a low TFT yield of 47 %. To improve the yield, we formed a trench structure to relieve the stress by etching the SiO_2 around the TFTs. As shown in Fig. 5(b), most of the wrinkles formed along the trenches between the TFTs, not on the TFTs. This improved the TFT yield (proportion of TFTs without wrinkles) from 47 % to 98 %.

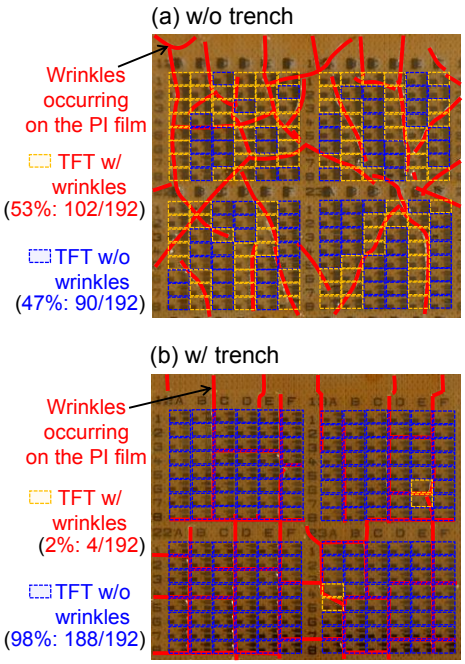

Fig. 5. Wrinkles on TFT array (192 TFTs) (a) with and (b) without trench structure of SiO_2 layer after the LLO process.

4 SUMMARY

We developed oxide TFTs that can be driven from the backside of a PI film substrate using 3D wires. Fabricated TFTs with L from 10 μm down to 3 μm exhibited clear switching behavior with an on/off current ratio of over 10^7. We also proposed a trench structure to suppress the influence of wrinkles that form on the TFT array. These developments are a step towards the realization of bezel-less flexible panel units.

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