Scan Driver Circuit for Suppressing Degradation of Pull-Down Units Using Depletion-Mode a-IGZO TFTs

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ABSTRACT

This paper proposes the scan driver circuit for depletion-mode a-IGZO TFTs using AC-driven CLK signals with the capacitive coupling effect for suppressing degradation of pull-down units. Simulation results show the proposed circuit generates stable output in the threshold voltage range from -2.0 V to +5.0 V.

1 Introduction

In the case of hydrogenated amorphous silicon (a-Si:H) thin-film transistors (TFTs) which have been widely used in liquid crystal display (LCD) panels, there was a stability problem due to threshold voltage (V_{th}) shift. And low-temperature polycrystalline silicon (LTPS) TFTs has arisen because it is suitable for current driving of active-matrix organic light-emitting diode (AMOLED) display. But the high cost of the ELA process and non-uniformity characteristics increase the demand for new materials. Among the candidates of materials, oxide TFTs have been intensively researched because of their good mobility and uniformity characteristics. However, a-IGZO TFTs have a depletion-mode characteristic and a negative threshold voltage, which cause current to flow even when the gate-source (V_{GS}) is 0 V [1]. When it is applied to integrated circuit structures such as scan drivers, leakage current paths may cause circuit malfunction. To solve this problem, many research teams have proposed a circuit to prevent leakage path by adding a lower gate low voltage (VGL) line, carry signal, and applying a series-connected two-transistor (STT) structure [2].

Meanwhile, the scan driver generates one output pulse for 1 line time (1H time). At this time, the output should not occur during the remaining time after the output period. For stable output, a pull-down unit is built-in to maintain the VOUT[n] as VGL excluding the output period [3]. In the display driving scan driver circuit, the pull-down unit is composed of TFTs. When the oxide TFTs are subjected to continuous electrical bias stress, the device characteristics change and degradation occurs, resulting in a V_{TH} shift problem [4, 5].

In this paper, we proposed a highly reliable scan driver circuit composed of a-IGZO TFTs considering a depletion-mode operation. In addition, the proposed circuit can suppress the degradation by AC driving of pull-down units using the capacitive coupling effect of the capacitor.

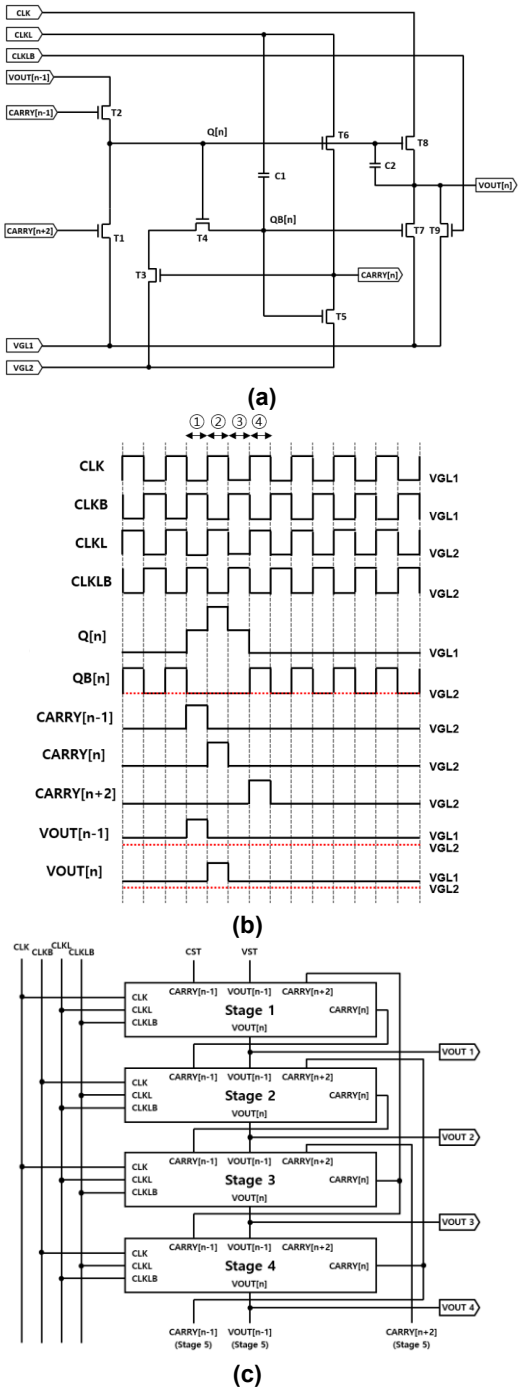


Fig. 1 Proposed scan driver circuit: (a) schematic, (b) timing diagram, and (c) block diagram.

2 Proposed Scan Driver Circuit

Fig. 1 (a) and (b) show the schematic and timing diagram of the proposed scan driver circuit. Also, Fig. 1 (c) shows the block diagram of the proposed circuit and the shift register operation of various stages. The proposed circuit consists of 9 TFTs and 2 capacitors. The circuit has 4 clock signals, which are two pairs of two-phase clocks with different low levels which are VGL1 and VGL2. The voltage range of CLK and CLKL is from -5 V to +28 V and from -13 V to +28 V, respectively. The drain and source of T7 and T9, which are TFTs included in the pull-down units, are connected to VOUT[n] and VGL1, respectively. The operation of the proposed scan driver circuit is divided into 4 periods.

2.1 Operation Process

A. Pre-charging Period

As CLKLB and VOUT[n-1] become VGH which means the high voltage, the Q[n] node voltage is charged up to VGH-V_{TH_T2} through T2. At this time, T8 and T6 are turned on by the Q[n] node, which pulls down VOUT[n] and CARRY[n] to VGL1 and VGL2, respectively. The QB[n] node has the VGL2 voltage due to the capacitive coupling effect of the CLKL signal and C1.

B. Bootstrapping Period

When CLKLB and CARRY[n-1] become VGL2, Q[n] goes to a floating state. At this time, as CLKLB and CLK become equal to VGH, Q[n] node is bootstrapped using C2. Thus, the driving capability of the pull-up TFTs, T8 and T6, is improved to transmit the output voltage to VOUT[n] and CARRY[n]. In addition, when the Q[n] node voltage has a voltage of VGH or higher, T4 is turned on and the CARRY[n] output occurs and T3 turns on, the QB[n] node is pulled down to VGL2. Since VGL2 voltage is applied to the gates of T7 and T9, stable VOUT[n] output is guaranteed.

C. Q[n] High Holding Period

When CLK and CLKL become VGL1 and VGL2 respectively, Q[n] node voltage is reduced to VGH by the capacitive coupling effect of C2. Then VOUT[n] and CARRY[n] output VGL1 and VGL2, respectively.

D. Reset and Low Holding period

As CARRY[n+2] becomes VGH, T1 is turned on, and as a result, the Q[n] node voltage is pulled down to VGL1. As Q[n] is discharged, T4 is turned off, and QB[n] has VGH voltage due to the capacitive coupling effect of CLKL and C1. Thereafter, QB[n] improves the degradation caused by bias stress while applying an AC driving voltage to the gate of T7 by CLKL and C1. Another pull-down TFT, T9, is also applied with an AC driving voltage by CLKLB. Therefore, the pull-down units discharge VOUT[n] with a 100% duty ratio enabling stable scan driver operation.

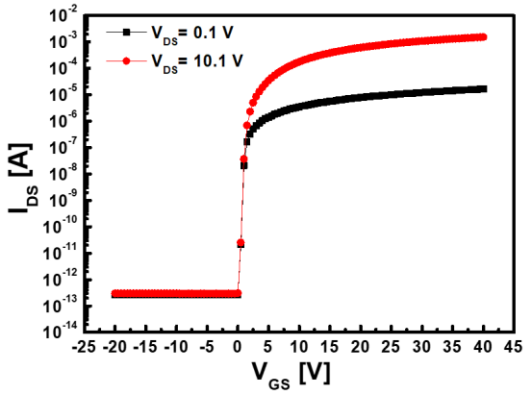


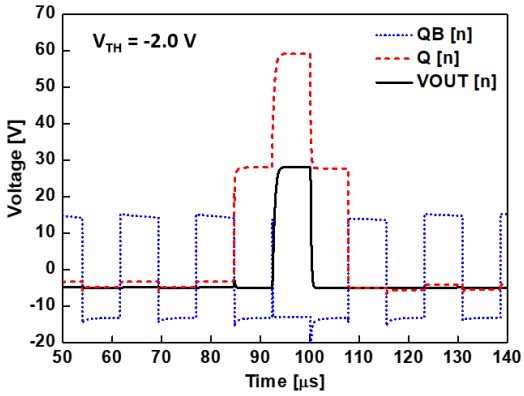
Fig. 2 I-V transfer characteristics of a-IGZO TFT.

2.2 Simulation

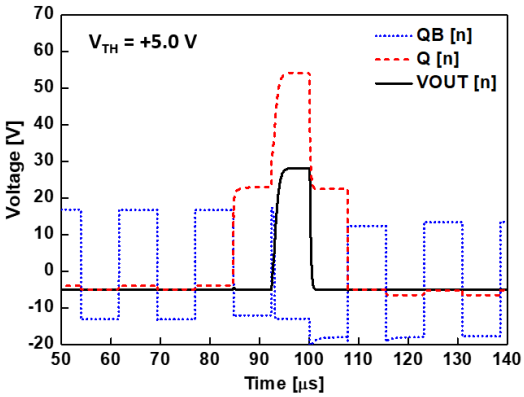
We simulated the proposed circuit using the circuit simulation program (Smartspice, Silvaco) with RPI (level = 35) model. We applied a 2 kΩ resistor and a 75 pF capacitor to each output terminal to evaluate the gate line load. The frame frequency was 60Hz, and the 1H time was 7.6 μs based on the UHD resolution display panel (3840 × 2160). All TFTs have a channel length of 5 μm. Fig. 2 shows the simulated I-V transfer curve of the a-IGZO TFT used in the proposed scan driver circuit. We controlled the V_{TH} in the simulation using V_{TH} parameters.

3 Results and Discussion

Fig. 3 shows the simulated voltage waveforms of Q[n], QB[n], and VOUT[n] nodes when the proposed circuit operated in depletion- (V_{TH} = −2.0 V) and enhancement- (V_{TH} = +5.0 V) modes. We confirmed the stable output of VOUT[n] in both depletion-mode and enhancement-mode. In Fig. 3 (a), the Q[n] node was fully charged to VGH which is pre-charge voltage. Also, the Q[n] node bootstrapping voltage reached +59.1 V with almost no loss despite having a negative threshold voltage. This result comes from the low leakage current at the Q[n] node. The QB[n] node voltage had VGL2 voltage when the Q[n] node voltage has VGH or higher, ensuring output stability. After the Q[n] High Holding Period, the Q[n] node voltage had VGL1 and the QB[n] had AC driving voltage using CLKL signal and C1. In Fig. 3 (b), unlike the depletion-mode operation, in the enhancement-mode operation, a pre-charge voltage equal to VGH-V_{TH_T2} was applied to the Q[n] node. Subsequently, the Q[n] node was bootstrapped to +54.2 V. Thus, the output pulse had a complete VGH voltage of +28 V. After the output period when Q[n] has VGL1, the QB[n] had an AC driving voltage. In conclusion, it was confirmed that the proposed circuit performs a stable operation for both depletion- and enhancement-mode a-IGZO TFTs.



(a)



(b)

Fig. 3 Simulated voltage waveforms of Q[n], QB[n], and VOUT[n]: (a) V_{TH} = -2.0 V, (b) V_{TH} = +5.0 V.

4 Conclusions

We proposed a reliable depletion-mode a-IGZO TFT-based scan driver circuit to suppressing the degradation of pull-down units. The proposed circuit can apply an AC driving voltage to the gate of each TFT by using the coupling effect of the CLK signal and the capacitor to relieve the bias stress applied to the T7 and T9 constituting the pull-down units. Accordingly, T7 and T9 each have a duty ratio of 50% and continuously discharge VOUT[n] in the period after the output. Also, the proposed circuit can eliminate the leakage current path that may occur at the Q[n] node by using VLG2, and thus it is confirmed that stable output is possible in both depletion- and enhancement-mode when the V_{TH} range is from -2.0 V to +5.0 V. Hence the proposed scan driver circuit can be adopted based on a UHD resolution display panel.

References

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