Alleviating Leakage Current by Adopting a Source-Follower Structure for AMOLED Displays of Wearable Applications

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ABSTRACT

In this work, an 8T2C pixel circuit is proposed for active matrix organic light-emitting diode (AMOLED) displays. The proposed circuit can compensate for VDD current-resistance drops, threshold voltage variations and leakage current of thin-film transistors. Simulation results demonstrate that the proposed circuit can achieve uniform display images for wearable devices.

1 Introduction

Owing to active-matrix organic light-emitting diode (AMOLED) displays' attractive characteristics, such as, high contrast ratio, wide color gamut, and flexibility, AMOLED displays are widely applied in consumer electronics [1], [2]. The OLED driving current is related to threshold voltage (V_{TH}) and source-to-gate voltage (V_{SG}) when the conventional pixel circuit composed of two thin-film transistors (TFTs) and one capacitor is utilized to drive OLEDs. However, the V_{TH} over the panel is not uniform when low temperature poly-silicon thin-film transistors (LTPS TFTs) are utilized for the backplanes [3], [4], [5]. Moreover, the current-resistance (I–R) drops on power lines directly influence the stored V_{SG} [6],[7]. Both circumstances lead to undesired OLED current (I_{OLED}) and non-uniform images. Several pixel circuits have been proposed to achieve display uniformity [8], [9], [10]. Nevertheless, the pixel circuits in [8] and [10] induce current flowing through OLEDs, which is the so-called image flicker. The flicker phenomenon will result in failure to display a whole black image, reducing the contrast ratio and increasing power consumption. The power consumption becomes a critical issue for AMOLED displays that offer excellent image quality, especially for wearable devices such as smartwatches which require thinness and lightweight characteristics. These requirements become the main constraint in wearable technology today equipping with limited battery capacity. To minimize the power consumption, a low-frame-rate technique is applied with reduced operating frequency which decreases the times of writing the display data and charging storage capacitors. The voltage at the gate node of driving TFTs must be maintained during the long-term emission period for providing stable images without brightness fluctuations. However, mobile devices adopt LTPS TFTs for AMOLED display backplanes because of their high mobility which shrinks the layout area with smaller required TFTs sizes. The high off current of LTPS TFTs yet leads to the failure of holding the gate voltage of driving TFTs in each pixel circuit, and a zero gray level cannot be maintained during the long-term emission period because of increasing V_{SG}. The defects cause decreased contrast ratio which is not desirable for AMOLED displays. Although the pixel circuits developed in [8], [9], and [10] compensate for V_{TH} variations and power supply I-R drops, none of these circuits have any leakage current compensation scheme for wearable AMOLED applications. Furthermore, the circuit proposed in [10] employed both n-type and p-type TFTs which increased fabrication process complexity and manufacturing costs. Therefore, a flicker-free pixel circuit is required that it consists of all p-type or n-type LTPS TFTs with the compensation scheme for V_{TH} variations and the leakage current issue.

This work demonstrates a pixel circuit consisting of eight p-type TFTs and two capacitors (8T2C) to deal with the problems aforementioned. The compensation structure ensures the accurate compensation of V_{TH} variations and VDD I-R drops, and effectively suppresses the voltage variation at the gate node of driving TFTs. The image flicker is suppressed by preventing any current from flowing through OLEDs. Simulation results show that the relative error rates are less than 5% when the V_{TH} of driving TFTs varies by ± 0.5 V and VDD drops by 0.5 V, simultaneously. The emission current fluctuation improves significantly compared with the conventional 4T2C circuit [8]. Therefore, the proposed circuit is able to provide accurate and stable emission currents for driving the low-frame-rate AMOLED displays with low power consumption.

2 Circuit Operation and Driving Scheme

2.1 Circuit Schematic and operation

Fig. 1 (a) shows the architecture of the proposed circuit with its timing diagram presented in Fig. 1 (b). The proposed circuit includes one driving TFT (T3), seven switching TFTs (T1, T2, T4, T5, T6, T7, and T8), two capacitors (C1 and C2), and four SCAN signals (S1[N-1], S1[N], S2, and EM). The operation of the proposed circuit can be divided into four periods as follows.

2.1.1. Reset period:

Initially, S1[N-1] is low to turn on T4. S2 and EM are low to turn on T1, T2, and T7. VSS is applied to node C through T7. The voltages at node A and node B are reset to VDD, simultaneously, so that the source-to-gate voltage (V_{SG}) of driving TFT, T3, is 0 V. T3 is thus turned off, preventing current from flowing through the OLED so that the image flicker is avoided.

2.1.2. Compensation period:

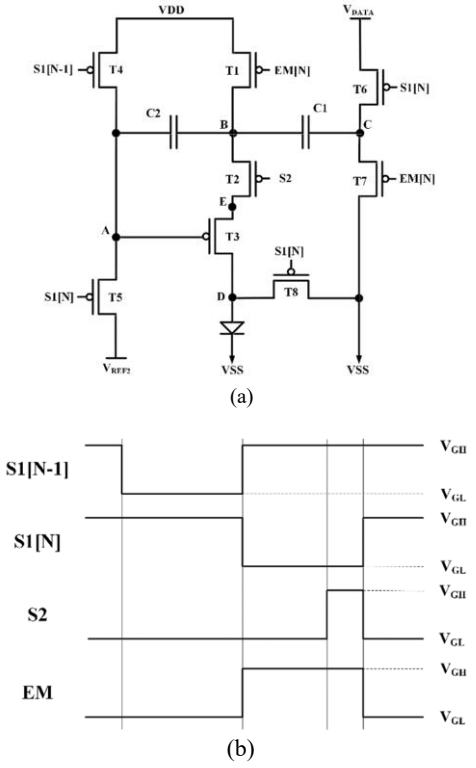

Fig. 1. (a) Schematic and (b) timing diagram of proposed pixel circuit.

TABLE I
PARAMETERS OF PROPOSED CIRCUIT

Parameter	Value	Parameter-	Value
V_{DD} (V)	3.3	$(W/L)_{T3}$ (μm)	3/22
V_{SS} (V)	-3.3	$(W/L)_{T1,T2,T4,T6\sim T8}$ (μm)	3/3
V_{DATA} (V)	4.5 ~ 5.95	$(W/L)_{T5}$ (μm)	3/3+3
V_{REF2} (V)	-1.95	C1 / C2 (pF)	0.35 / 0.35
V_{REF} (V)	4.65	$(W/L)_{TOLED}$ (μm)	3/22
SCAN (V)	5 / -4	C_{OLED} (pF)	0.2

S1[N-1] and EM goes high to turn off T1, T4, and T7, while S1[N] goes low to turn on T5, T6, and T8. S2 remains low to turn on T2. Therefore, the pixel circuit forms a source-follower type connection where the gate voltage of the driving TFT is set to V_{REF2}. Meanwhile, node B starts to discharge through T2, T3, and T8 until T3 turns off. Finally, the voltage at node B (V_B) will be discharged to $V_{REF2} + |V_{TH}|$, where V_{TH} is the threshold voltage of the driving TFT, T3. The voltage of node C (V_C) is kept at V_{REF} supplied by V_{DATA} through T6. In addition, V_D, which is the anode voltage of the OLED, is reset to VSS, and that the voltage across the OLED is 0 V, which is smaller than the V_{TH} of the OLED, 2.84 V. The OLED is thereby turned off to prevent flicker.

2.1.3. Data input period:

During this period, S2 becomes high to turn off T2. Data voltage (V_{DATA}) is input to node C through T6. By charge conservation, V_B is boosted to the voltage as presented in the following equation:

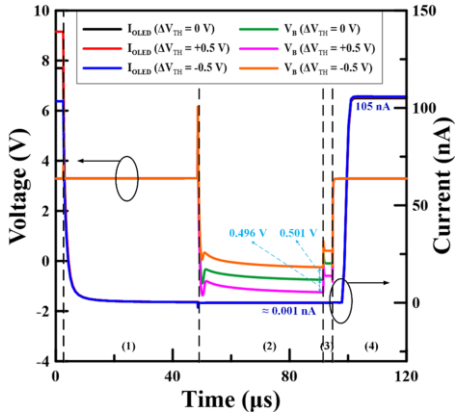

Fig. 2. Transient waveforms of node B and OLED emission current of proposed circuit as V_{TH} varies ±0.5 V.

$$V_B = V_{REF2} + |V_{TH}| + \frac{C1}{C1+C2}(V_{DATA} - V_{REF}) \quad (2.1)$$

Therefore, the V_{SG} of T3 is stored by C2, as shown in the following equation:

$$V_{SG} = V_{REF2} + |V_{TH}| + \frac{C1}{C1+C2}(V_{DATA} - V_{REF}) - V_{REF2}$$
$$= |V_{TH}| + \frac{C1}{C1+C2}(V_{DATA} - V_{REF}) \quad (2.2)$$

Notably, T2 is turned off in this period to prevent the stored voltage at the source node from discharging through T3 because the voltage shown in Eq. (2.2) will turn on T3. Owing to the high mobility of LTPS TFTs, the high discharging current will result in unexpected V_{SG} that cannot successfully compensate for V_{TH} variations.

2.1.4. Emission period:

S1[N-1] and S1[N] are high to turn off T4, T5, T6, and T8. S2 and EM go low to turn on T1, T2, and T7. The V_{SG} of T3 remains the same voltage as Eq. (2.2). The emission current (I_{OLED}) can be calculated as the following equation:

$$I_{OLED} = \frac{1}{2}k\left(\frac{W}{L}\right)(V_{SG} - |V_{TH}|)^2$$
$$= \frac{1}{2}k\left(\frac{W}{L}\right)\left\{VDD - \left[VDD - |V_{TH}| - \frac{C1}{C1+C2}(V_{DATA} - V_{REF})\right] - |V_{TH}|\right\}^2$$
$$= \frac{1}{2}k\left(\frac{W}{L}\right)\left[\frac{C1}{C1+C2}(V_{DATA} - V_{REF})\right]^2 \quad (2.3)$$

where k is $\mu_p \cdot C_{OX}$ and W/L is the aspect ratio of the TFT. Since V_{TH} and VDD are eliminated in Eq. (2.3), the pixel circuit can achieve uniform display images without the influences of V_{TH} variations of driving TFTs and VDD I–R drops.

2.2 Leakage compensation mechanism

In the pixel circuit, T4 and T5 form a compensation structure to keep the voltage at node A (V_A) stable during the emission period. To achieve this purpose, there are two

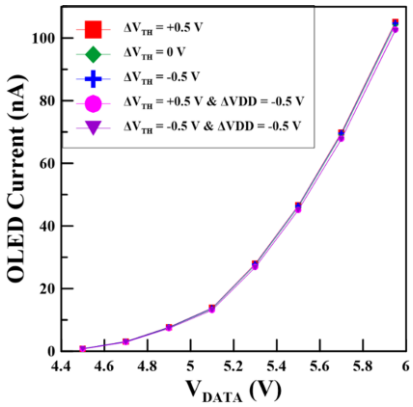

Fig. 3. Transient waveforms of node B and OLED emission current of proposed circuit as V_{TH} varies ±0.5 V.

leakage current paths applied to node A. One is the leakage current generated by T5, $I_{Leakage}$, which flows from node A to V_{REF2}, thereby discharging the node A. Meanwhile, a compensation current (I_{Comp}) is generated by T4, which flows from VDD to the node A to charge C1. Consequently, the voltage drops at the node A caused by $I_{Leakage}$ are reduced by the employment of I_{Comp}. In addition, the magnitude of the leakage current is decided by the V_{DS} of T4 or T5, which means that the leakage compensation can be optimized by adjusting the voltage level of VDD or V_{REF2}. Under this circuit design, the leakage compensation can achieve a balanced situation at a certain gray level. Therefore, the proposed pixel circuit works functionally and provides stable images at low-frame-rate operation, verifying the capability of applying to low-frame-rate AMOLED displays.

3 Results and Discussions

This circuit conducts HSPICE simulation to verify the feasibility and the performance of the proposed circuit. The simulation is for a 1.41 inch panel, whose frame rate and resolution are 15 Hz and 320×360, respectively. The compensating period is set to 46 µs. The simulated parameters of TFTs, capacitors, scan signals, and power supplies are listed in Table I. Fig. 2 plots the simulated transient waveforms of V_B and OLED emission current (I_{OLED}) when threshold voltage (V_{TH}) varies ±0.5 V. The simulation results show that the differences between the V_B are 0.501 V and 0.496 V, which nearly match the 0.5V variations of V_{TH}. Furthermore, I_{OLED} is close to 0.001 nA before the emission period, achieving a flicker free and whole black display images and thus enhancing the contrast ratio. Fig. 3 demonstrates the OLED emission current when V_{TH} varies ±0.5 V and VDD drops 0.5 V, and the current is nearly identical at each data voltage. Figs. 4 (a) and (b) show the relative error rates under the condition of V_{TH} variations and VDD I–R drops. In Fig. 4 (a), the current error rates are all below 4.2% within the whole data rage when V_{TH} varies ±0.5 V. Furthermore, the current error rates concerning the power line I–R drops and V_{TH} variations simultaneously are under 5% as shown in Fig. 4 (b). Hence, the simulation results mentioned above demonstrate that the proposed pixel circuit can provide

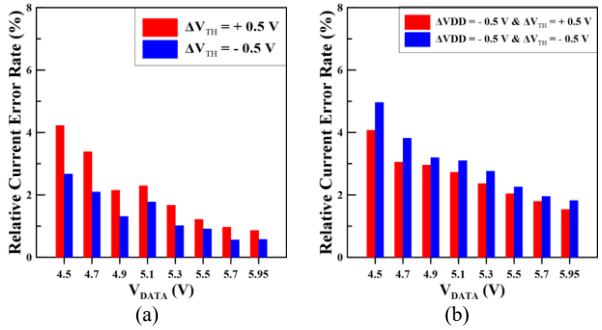

Fig. 4. Relative current error rates when (a) ΔV_{TH} is ±0.5 V (b) ΔV_{TH} is ±0.5 V and VDD I–R drop is 0.5 V.

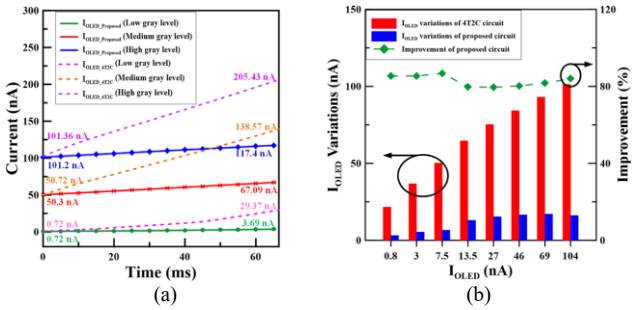

Fig. 5. (a) Variations of OLED current during emission period (b) I_{OLED} variations improvement compared with 4T2C circuit [6].

uniform OLED driving current with the effective compensation of V_{TH} variations and VDD I–R drops. To verify the functionality of leakage current compensation, Fig. 5 (a) plots the current increased during the emission period of the proposed circuit and the 4T2C circuit [6] Since the proposed circuit employs a leakage current compensation structure, it displays a relative lower emission current increase which is 2.97 nA, 16.79 nA, and 16.2 nA at the low, medium, and high gray level, respectively. In addition, Fig. 5 (b) plots the improvements of OLED driving current increased during the 66.6 ms emission period. The improvements are calculated as the following equation:

$$\text{Improvement}(\%)=\frac{\Delta I_{OLED\_4T2C}-\Delta I_{OLED\_8T2C}}{\Delta I_{OLED\_4T2C}} \quad (3.1)$$

The leakage current improvements over the entire gray level range are greater than 79%. These verification results confirm the feasibility of low-frame-rate operation utilizing the proposed circuit, which is suitable for wearable device applications with low-frame-rate operation

4 Conclusions

This work proposes an 8T2C circuit for AMOLED displays, which effectively compensates for V_{TH} variations, VDD I–R drops, and leakage phenomenon. Simulation results verify that the proposed circuit executes effective compensation for V_{TH} variations in LTPS TFTs and I–R drops in power lines. The flicker phenomenon is also suppressed with the VSS applied at the anode of OLEDs. Moreover, the proposed circuit shows

that the current increased during the long-term emission period is alleviated compared with the 4T2C circuit [6]. Therefore, the proposed circuit is able to achieve high contrast ratio and provides uniform display images for wearable devices.

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