Selective Doping in Drain Region of Amorphous Oxide Thin-Film Transistor by Electrical Stress under Illumination

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ABSTRACT

A unique method to enhance the electrical performance of oxide thin film transistor(TFT) is presented. Photo-induced holes and positively charged oxygen vacancies are attracted to near the drain terminal by applying negative bias to gate and drain electrode under illumination. These positive charges gather electrons to form n+ doped region and thus lower the parasitic resistance. The field-effect mobility (μ_{sat}) increased up to 80% via this electrical forming method.

1 Introduction

It is well known that negative bias illumination stress (NBIS) causes trapping of photo induced positive charges at the interface between gate insulator and semiconductor in oxide TFTs [1-2].

We also apply negative bias at the drain terminal during the NBIS test to collect the positive charges at there. It is expected that the trapped positive charges attract the free electrons in the oxide semiconductor to near the drain part. The gathered electrons form n+ doped region which is similar to implanted source/drain of silicon TFTs as depicted in Fig 1.

2 Experiment

We fabricated a top gated a-IGZO TFT with bottom contact configuration on glass substrate. Firstly, 150nm thick indium tin oxide (ITO) film was sputtered for source/drain electrode and then patterned using wet etching process. Secondly, 30nm-thick a-IGZO film was also sputtered as an active layer followed by deposition of 9nm thick Al_2O_3 layer using atomic layer deposition technique. After that, a-IGZO/Al_2O_3 bilayer was etched with diluted HF and next was covered with 176nm thick Al_2O_3 layer. Lastly, gate electrode was formed in the same way as source (S)/drain (D) electrode.

3 Results

Fig 2(a) and (b) show the changes in transfer characteristic and μ_{sat} respectively during the 2 hours of NBIS without applying negative drain bias (V_G = -20V, V_{DS} = 0V). A large shift in V_{th} and negligible change in μ_{sat} were observed. On the contrary, when the device was subjected to negative drain bias under NBIS condition (V_G=V_{DS} = -20V), a small V_{th} shift and significant increase in μ_{sat} were observed as shown in Fig 2(c) and (d) respectively.

4 Discussion

We speculated that the reduction of parasitic resistance (R_P) due to the formation of highly doped region is the direct cause of the enhanced field-effect mobility. To evaluate the R_P, we used gated-transmission line method (TLM). The total drain to source resistance (R_{tot}) of a TFT operated in a linear region can be expressed as follows [3],

$$R_{tot} = R_{ch} + R_P \quad (1)$$

$$= L/W\mu_{FEi}C_g(V_{GS}-V_{th}-V_{DS}/2) + R_p \quad (2)$$

where L, W, μ_{FEi} and C_g are channel length, channel width, intrinsic mobility and gate capacitance, respectively. Fig 3 shows the measured R_{tot} for various L under the same bias condition (V_{GS}-V_{th} = 10V, V_{DS} = 0.1V) and identical channel width of 40μm. By fitting a line to this plot of R_{tot} versus L, we can obtain R_p according to the equation (2). The extracted R_p was 9430 Ω for the pristine state and this is comparable to the reported value. It is well known that the R_p comes from the resistive region of bulk AOS and S/D contacts in the conventional inverted staggered TFTs or top gated TFTs having bottom contact configuration like the tested device herein [4].

We also performed the same procedure to evaluate the R_p of the device which is treated by the proposed doping method. After the doping process, the R_{tot} decreased for all channel lengths as shown in Fig 3. However, no y-intercept was found unlike the untreated case. This means that effective channel length becomes shorter than mask length due to the increase in carrier concentration near the drain part as depicted in Fig 4.

Another solid evidence for the selective doping was found in capacitance-voltage (C-V) measurements. Figure 5(a) and (b) show the gate-to-drain capacitance (C_{GD}) and gate-to-source capacitance (C_{GS}) respectively. After the doping process, the C_{GD} under negative gate bias nearly doubled while the C_{GS} was almost unchanged. This is due to the local increase in doping density and consequential reduction in thickness of depletion layer as stated earlier. Note that, this increased capacitance and μsat have remained stable even after two months past from the day we had treated the device.

5 Conclusions

Selective doping is accomplished by applying

negative drain bias during NBIS test. The reduction of contact resistance is confirmed by TLM analyses.

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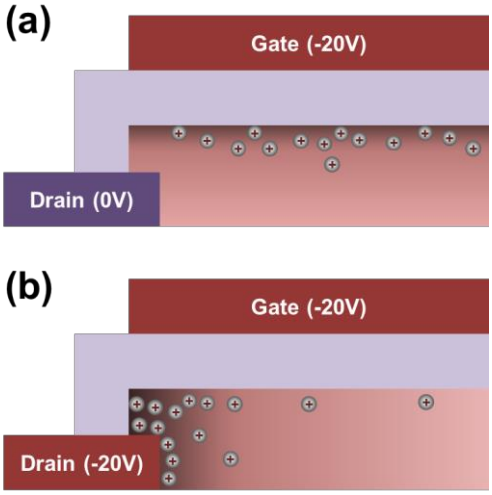

Fig. 1 Schematics illustrating distribution of positive charges inside a-IGZO under NBIS condition with drain bias of (a) 0V and (b) -20V

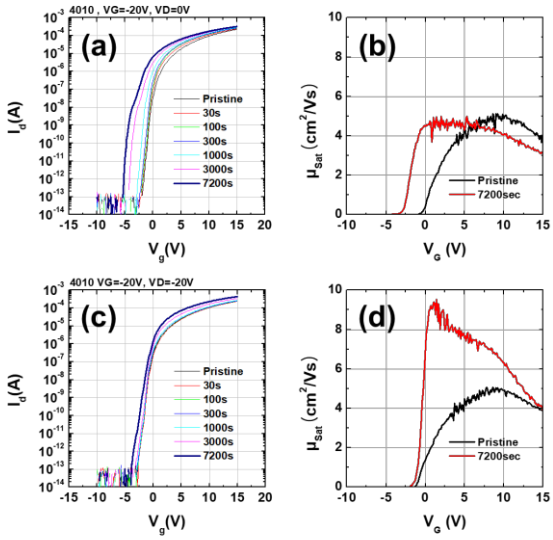

Fig. 2 Evolutions of transfer characteristics under NBIS condition with drain bias of (a) 0V and (c) -20V as a function of test time. (b) and (d) are the changes in saturation mobility obtained from (a) and (c), respectively.

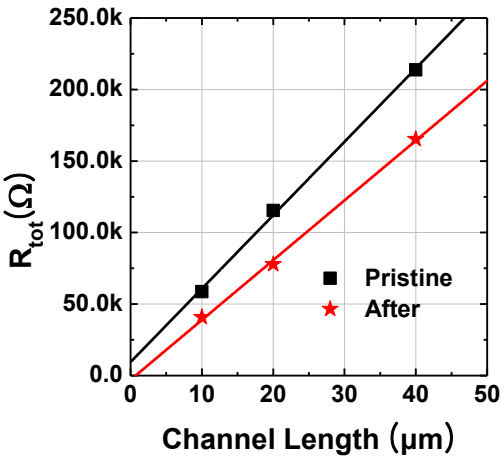

Fig. 3 Plots of R_{tot} as a function of the channel length for pristine state and doped device via proposed method.

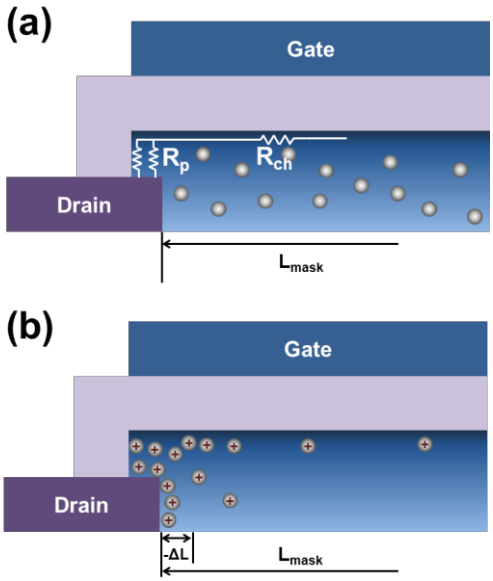

Fig. 4 Schematic diagrams of resistance elements in a top-gated TFT having bottom contact configuration with (a) un-doped and (b) doped drain region

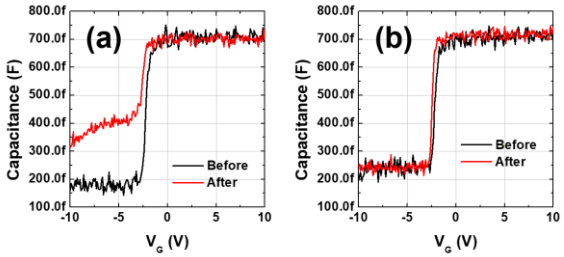

Fig. 5 (a) Gate to drain and (b) gate to source capacitance as a function of gate bias before and after the doping process