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Investigation of NBIS Degradation Mechanism in Oxide TFT Assisted by Charge Trap Phenomena

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ABSTRACT

IGZO-TFT with CTL was designed to understand the degradation mechanism of NBIS. The TFT showed stable retention characteristics after applying negative V_g with light irradiation. It shows that positive charge is injected to CTL through the tunneling layer. It is suggested that holes are the possible origin of NBIS degradation.

1 INTRODUCTION

In 2004, the first thin-film transistor (TFT) using an amorphous oxide semiconductor (AOS) as the channel layer was reported [1]. AOS materials, such as In-Ga-Zn-O (IGZO), are characterized by a low process temperature below 400ºC, high-mobility over 10 cm^2/Vs, large area uniformity, and high-transmittance to visible light. It has attracted much attention as a channel material for TFTs in flat panel displays (FPDs). The instabilities of threshold voltage (V_{th}) under gate voltage (V_g) stress and light irradiation such as positive bias stress, positive bias and temperature stress, constant current stress, and negative bias and light illumination stress (NBIS) are issues. The V_{th} shift due to NBIS degradation is the most serious degradation mode for TFTs in liquid crystal displays. The reason is that most of their operating time is spent with negative V_g application, and they are exposed to light irradiation from the backlight. Generally, V_{th} in AOS-TFT is stable against negative bias stress [2]. On the other hand, it is known that V_{th} shifts in negative direction when NBIS is applied.

To solve this problem, degradation phenomena induced by NBIS, and physical models are discussed. Several models of NBIS degradation have been reported including the trapping of holes generated by light irradiation to the interface between channel and gate insulator [2], positively charged oxygen defects [3], metastable O-O bond [4], and bistable hydrogen [5]. Elucidating the degradation mechanism of NBIS is an important research because it will directly lead to the improvement of reliability and performance of AOS-based displays.

In this work, we focused on use of charge-trap memory structure to elucidate the degradation mechanism of NBIS in oxide TFTs. The charge-trap memory has a structure in which a charge trap layer (CTL) is inserted between the blocking layer and the tunnel layer (TL). Erase and program operations are carried out by carrier tunneling through the TL. Electrons and holes can easily pass through the TL and inject to the CTL. Therefore, we consider that charge-trap memory structure can be separated from oxygen defects, oxygen and hydrogen atoms, which are candidates for the cause of NBIS.

Charge-trap memories using oxide semiconductor channels demonstrated electrical program operations with positive bias to control-gate by electron injection into charge trap layer such as SiN_x; however, they cannot be erased electrically by negative bias to control-gat [6]. The poor erase operation is attributed to the physical property that AOS has difficulty in generating holes. To achieve erase operation, a negative bias application with light irradiation is essential method. This erase operation is described by photo-induced hole generation from localized defect in channel layer and its hole injection into the CTL [6]. Remarkably, the erase condition in charge-trap memories is almost same as NBIS environment in TFT for display. Thus, we consider that investigation of the erase characteristics under light irradiation of oxide TFT with CTL can contribute understanding origin of positive charge and mechanism of negative V_{th} shifts under NBIS. In this work, we describe an interesting method assisted by charge-trap phenomena in gate stack for degradation analysis of NBIS for oxide TFTs.

2 Experiment

2.1 MOS capacitor

At first, we measured the charge-trap properties of HfO_2 using metal-oxide-semiconductor (MOS) capacitor. For the sample fabrication, 30-nm-thick HfO_2 was deposited on a Si substrate (p-type) with 3.5-nm-thick thermally oxidized-SiO_2 by RF magnetron sputtering. 20-nm-thick SiO_2 was deposited by plasma-enhanced chemical vapor deposition (PECVD) with tetraethoxysilane (TEOS) as a TL. Al thin films were used as electrodes on both top and bottom sides. As a comparison, we also fabricated a sample with only TEOS-SiO_2 (30 nm) deposited on a Si substrate (inset of Fig.1).

2.2 TFT

In this work, we used amorphous IGZO (a-IGZO) as a channel and fabricated TFTs with TL-SiO_2 and CTL-HfO_2 structures as shown in Fig. 2. The 30-nm-thick HfO_2 was deposited on a Si substrate with 20-nm-thick thermally oxidized-SiO_2 by RF magnetron sputtering. 5-nm-thick SiO_2 for the TL was deposited by PECVD. In addition, 70-nm-thick a-IGZO (In:Ga:Zn=2:2:1 at%) was deposited as the channel by RF magnetron sputtering. Pt/Mo stacked film was used as source/drain electrodes. The device structure was formed by photolithography, wet-etching, and lift-off methods. IGZO-TFTs with TEOS-SiO_2 (5 nm) / thermally oxidized-SiO_2 (20 nm) gate insulator without CTL was also fabricated as a reference. For the light irradiation, we used a xenon light source and a monochromator, and the light intensity was adjusted to 90 μW/cm² in the wavelength range of 400 to 600 nm.

3 RESULTS AND DISCUSSION

3.1 *C-V* characteristic of MOS capacitor

The capacitance-voltage (*C*-*V*) characteristics of each capacitor are shown in Fig. 1. For hysteresis measurement, the V_g was swept from the forward direction ($-V_g$ to $+V_g$) to the reverse direction ($+V_g$ to $-V_g$). It was confirmed that the *C*-*V* characteristics of the capacitor without HfO_2 layer did not have hysteresis. On the other hand, a hysteresis width of 0.57 V was confirmed when HfO_2 was inserted as CTL. Therefore, it was confirmed that the HfO_2 worked as a charge-trapping layer [7].

3.2 Charge trap property in IGZO TFT under negative-bias illumination

TFT with the CTL structure as shown in Fig. 2 was fabricated, and their program/erase characteristics were evaluated. For program, V_g of +10 V was applied for 1 s. For erase, V_g of -10 V was applied. For light irradiation, light at 400 nm (3.1 eV) was used.

Figure 3 (a) shows the transfer characteristics of before and after program and erase operations. From Fig. 3, V_{th} was shifted in the positive direction compared to the initial value. This result suggests that the electrons were injected into CTL-HfO_2 when V_g of +10 V was applied. However, the V_{th} did not return to the initial value even erase time was increased from 1s to 50 s (w/o light irradiation), as shown in Fig. 3. This result indicates that injected electrons in CTL-HfO_2 are not released, or holes are not injected from the IGZO channel into CTL-HfO_2 under the negative V_g. Similar behavior has been reported in other reports [8-11].

In contrast, a light irradiation has been reported to perform erase operation of IGZO-based charge trap memory [6]. In this research, 400 nm light was used to irradiate the IGZO memory device, and at the same time, V_g of -10 V was applied for 50 s. Then, V_{th} shifted from the programmed state to the negative direction (Fig. 3). The V_{th} was on the negative V_g side compared to the initial value. If the injected electrons in CLT-HfO_2 are released by light, the V_{th} should return to the initial value. However, V_{th} was more negative V_g side than the Initial V_{th}, there is a possibility that positive charges such as holes were injected into CTL-HfO_2. Figure 4 shows the dependence of photon energy on the V_{th} shift of IGZO-TFT with CTL and without CTL. For the TFT with CTL, the V_{th} shift increases at higher photon energy compared to TFT without CTL.

AOS-TFTs tend to show V_{th} shift in negative direction under NBIS from the initial value. The NBIS degradation is attributed to the localized defect in the band gap of IGZO and considered to be caused by the high-density localized defect above the valence band [12]. According to the proposed model [13], light irradiation excited electrons from this defect and generates holes. These holes are trapped at the interface between channel and gate insulator by the negative V_g. In our case, the holes generated by photo-irradiation in a-IGZO diffuse to the interface between a-IGZO and SiO_2 by negative V_g. The holes pass through the TL and can be injected into CTL-HfO_2. In other words, the negative shift of V_{th} caused by erasure operation can be explained by hole injection into CTL-HfO_2.

3.3 Comparison of charge retention characteristics and discussion of NBIS degradation mechanism

From section 3.2, the program and the erase operation using light were confirmed. If the negative V_{th} shift is attributed to injected hole into CTL, V_{th} is expected to remain unchanged over time without bias and to maintain a memory window between the programmed and erased states. This means non-volatility in memory. Non-volatility can be confirmed by the retention characteristics. In other words, the injected positive charge into the CTL is considered to be a hole, when sufficient retention property at erased state are obtained.

Figure 5 (a) and (b) shows the retention characteristics for TFT with and without CTL, respectively. After applying V_g of +10 V for 1 s as program, the drain current (I_{ds}) was measured under the condition of V_d = 0.1 V with V_g = 0 V. For the evaluation of erase characteristics, V_g of -10 V was applied for 50 s with 400 nm (3.1 eV) light irradiation, and then the I_{ds} value was read out under the same conditions of V_d = 0.1 V and V_g = 0 V. The bias condition on the erase operation corresponds to the NBIS environment.

The I_{ds} on the program side does not increase with time in both the structures with and without CTL, as shown in Fig. 5 (a) and (b). The TFT with CTL continues to hold positive charge because the I_{ds} on the erase side does not decrease rapidly. On the other hand, Fig. 5 (b) shows that for the TFT without CTL, the I_{ds} on the erase state decreases to an order of magnitude close to that of the program state in 10^3 s. These results show that positive charge is released in a relatively short time in TFT without CTL sample.

In the case of NBIS degradation in AOS-TFTs, it was reported that the trapped positive charge at the interface between channel and SiO_2 insulator is released in a short time, and the I_{ds} value is decreased [14]. Therefore, the difference in the positive charge retention property of the TFT with CTL suggests that the positive charge is injected into the CTL-HfO_2 through the TL by applying a negative V_g under light irradiation. If the positive charge is not a hole but hydrogen or oxygen-related defects, it is difficult to explain the injection of positive charge into CTL through the TL. Based on these results, we consider that the hole generation from the localized level in the IGZO is the possible origin of the NBIS degradation.

4 Conclusions

In this research, we designed an IGZO-TFT with CTL to understand the cause of degradation mechanism of NBIS. The IGZO-TFT with CTL showed longer retention time than the TFT without CTL after applying V_g with light irradiation. From the above results, it can be concluded that positive charge is injected into the CTL. Therefore, it is suggested that hole generation is the possible origin of the NBIS degradation.

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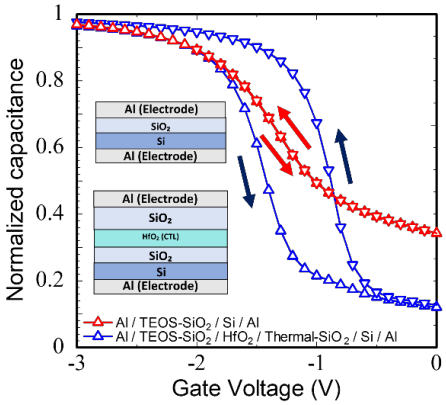

Fig. 1 *C-V* characteristics of MOS capacitors with and without CTL.

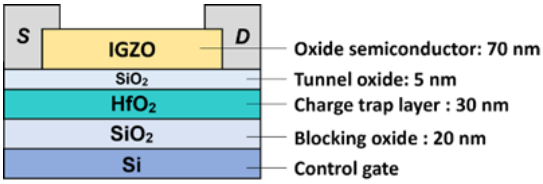

Fig. 2 Charge trap memory structure.

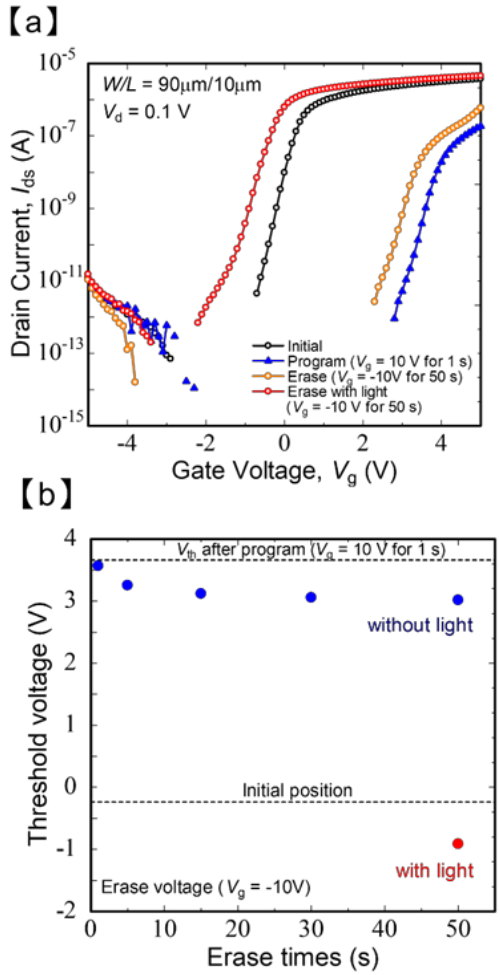

Fig. 3 (a) Transfer characteristics of the IGZO-TFT with CTL. (b) V_{th} shift of the IGZO-TFT with CTL. V_{th} was estimated from V_g at I_d = 1 nA.

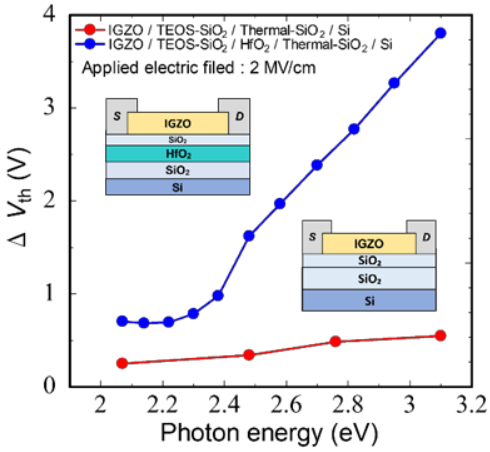

Fig. 4 Influence of photon energy at erase condition. The ΔV_{th} was calculated from the difference of V_{th} between program and erase state.

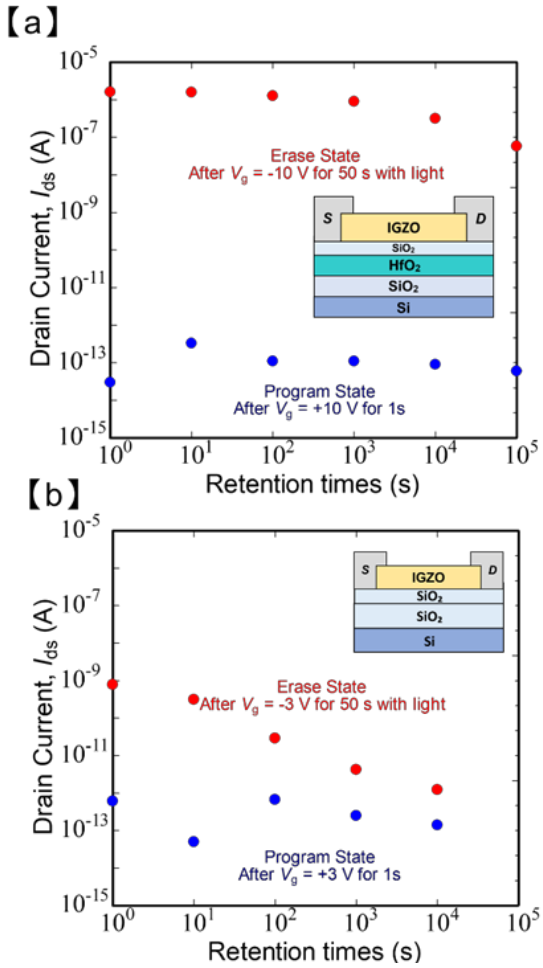

Fig. 5 Retention characteristics of the IGZO-TFT (a) with and (b) without CTL. The bias condition on the erase operation corresponds to the NBIS environment.