An Integrated Scan Driver Circuit for Picture Quality and Uniformity Improvement of OLED Display

Eun Kyo Jung, Yong-Hoo Hong, Hwarim Im, and Yong-Sang Kim

Email : yongsang@skku.edu, yskim651@gmail.com
Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, Korea
Keywords: OLED, LTPS TFT, Scan Driver Circuit, Black Data Insertion, External Compensation

ABSTRACT

We propose a novel integrated scan driver circuit. The proposed circuit can generate simultaneously the scan output for data addressing and black data insertion as well as sense output for the external compensation. The simulation results verified the stable operation during the 1H time.

1 Introduction

Low-temperature poly-Si (LTPS) thin-film transistors (TFTs) have been widely used as backplane technology in mobile and compact display because of their high mobility, excellent stability, and fast response speed compared to hydrogenated amorphous silicon (a-Si:H) TFT and amorphous indium gallium zinc oxide (a-IGZO) TFT [1-2]. However, LTPS TFT has non-uniform characteristics, which cause the threshold voltage (V_{th}) and mobility variation during excimer laser annealing (ELA) process [3]. The V_{th} can be shifted by continuous bias stress, which can lead to a serious OLED malfunction. Thus, the V_{th} and mobility compensations of TFT should be achieved to gain good uniformity in the display. Above of all, the higher the resolution, the smaller the pixel size, so the external compensation method is essential [4-5].

Meanwhile, the active-matrix organic light-emitting diode (AMOLED) displays have high brightness, a wider viewing angle, and uniform luminance than liquid crystal display (LCD). Despite these outstanding merits, the OLED displays still have issues of picture quality such as motion blur and flicker phenomenon [6]. To improve these problems, various companies and laboratories have applied the black data insertion method and high refresh rates such as 120 Hz and 240Hz [7].

Thus, we propose an integrated scan driver using black data insertion to suppress picture quality deterioration. In addition, the proposed circuit can realize the sense[n] output waveform to compensate for driving TFT of pixel circuit as well as scan[n] output waveform.

2 Pixel Circuit for External Compensation

Fig 1. (a) is the pixel circuit (3T1C) based on LTPS TFT. The T1 is the driving TFT for grayscale representation. The T2 and T3 are switching TFTs for data insertion and electrical characteristic compensation of T1, respectively. Fig. 1 (b) exhibits the timing diagram is composed of data addressing, black data insertion, and sensing operations, respectively. By applying these operations to the pixel circuit, the picture quality and uniformity for the OLED display can be improved.

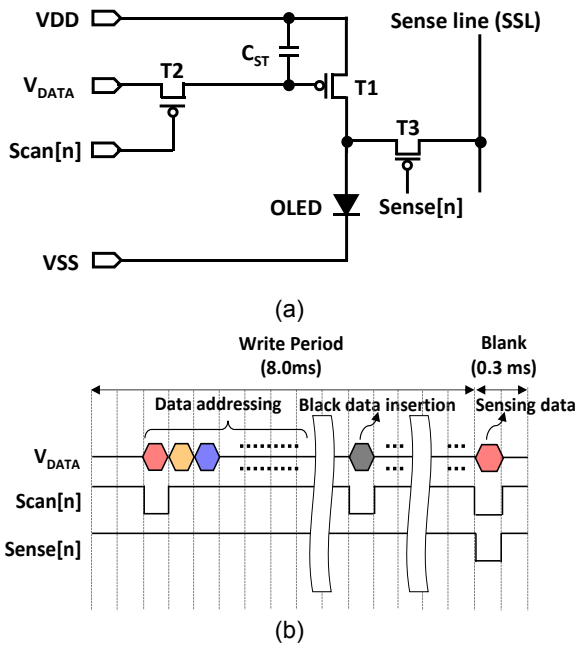
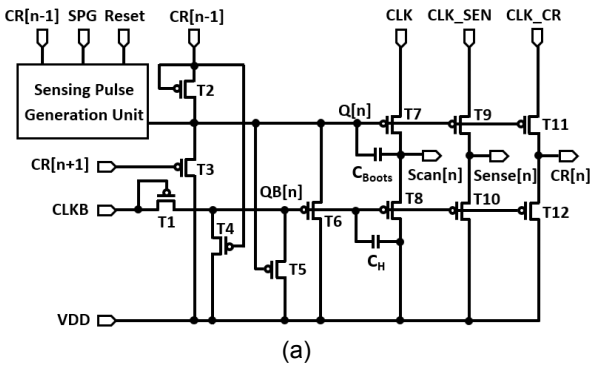


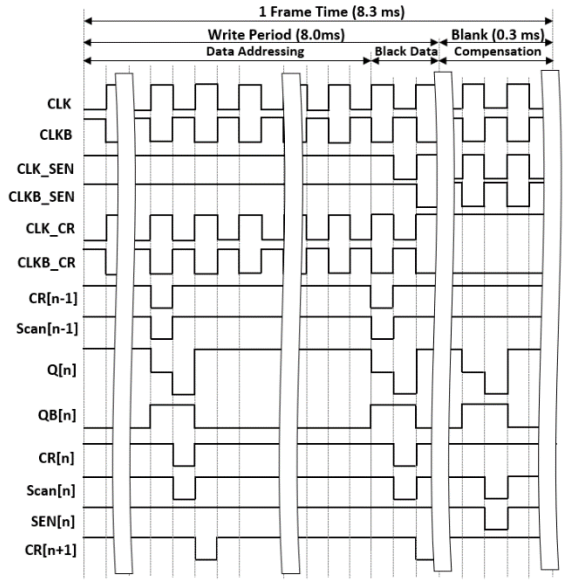
Fig. 1 Pixel circuit structure (a) circuit schematic (b) timing diagram for 1 frame time (8.3 ms).

3 Proposed Scan Driver Circuit

Fig. 2 (a) and (b) exhibit the circuit schematic and timing diagram of the proposed scan driver circuit. The proposed circuit composes of 18 TFTs and 3 capacitors. To output Sense[n] waveform, we designed the sensing pulse generation unit (SPGU) as shown in Fig. 2 (a). The sensing waveform output method randomly outputs the waveform of one gate line for 1 frame time. Therefore, SPGU consists of a signal that selects one arbitrary line and a signal that pre-charges and resets the Q node. The circuit has 6 clock signals, which are three pairs of two-phase clocks. The voltage range of CLK, CLK_SEN, CLK_CR is from -5V (VGL) to +15V (VGH). The operation of the proposed scan driver circuit is divided into 3 periods as shown in Fig. 2 (b). The circuit operation is as follows.



(a)



(b)

Fig. 2 Proposed scan driver circuit : (a) circuit schematic, (b) timing diagram.

3.1 Operation Process

A. Data Addressing Period (Scan[n] output)

When CLKB and CR[n-1] become VGL which means the low voltage, the Q[n] node voltage is discharged up to VGL+V_{th_T1} through T2. At this time, T7, T9, and T11 are turned on by the Q[n] node, which pulls up Scan[n], Sense[n], Carry[n] to VGH. The QB[n] node has the VGH since T4 and T5 are turned on. Next, When CLKB and CR[n-1] become VGH, Q[n] goes to a floating state. At this time, the CLK become equal to VGL and Q[n] node is bootstrapped using C_{Boots}. Thus, the driving capability of the pull-down TFTs, T7 and T11, is improved to transmit the output voltage to Scan[n] and CR[n]. At this time, Sense[n] has the VGH through CLK_SEN and T9. As CR[n+1] becomes VGL, T3 is turned on, and as a result, the Q[n] node voltage is pulled up to VGH. At this time, CLKB has a VGL and QB[n] node voltage is pulled down to VGL. Thus, Scan[n], Sense[n], and CR[n] are pulled up to VGH. The QB[n] node voltage maintains VGL during the next 1H time through a holding capacitor (C_H).

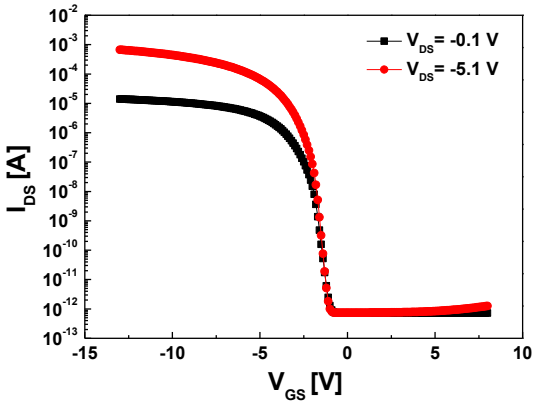


Fig. 3 I-V transfer characteristics of LTPS TFT.

B. Black Data Period (Scan[n] output)

When the emission duty is achieved to 50%, CR[n-1] and CLKB become VGL and the Q[n] goes to a VGL+V_{th_T1} through T2. After this time, the operation Is completely the same as *A* of the operation process.

C. Compensation Period (Scan[n]/ Sense[n] output)

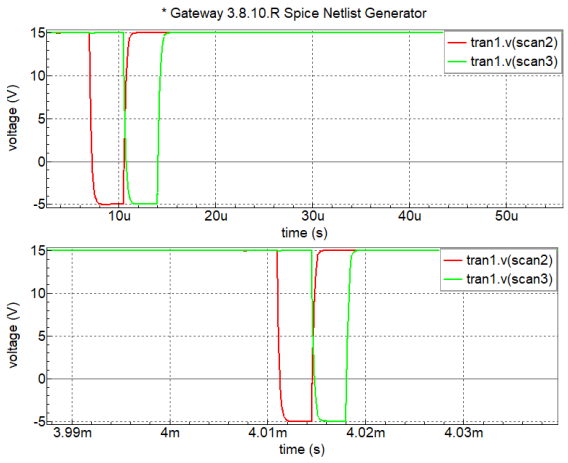
When the black period is reached, the Q[n] node voltage is discharged up to VGL+V_{th_T1} through selection pulse generation (SPG) signal of SPGU. We applied a 0.2 kΩ resistor and a 30 pF capacitor to each output terminal to evaluate the gate line load. After this period, the CLK become equal to VGL and Q[n] node is bootstrapped using C_{Boots}. At this time, Scan[n] and Sense[n] has the VGL through CLK and CLK_SEN, respectively.

3.2 Simulation

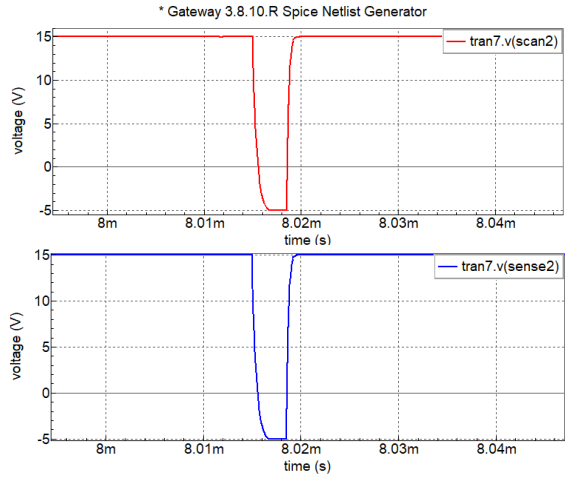
We simulated the proposed scan driver circuit using the Smartspice simulation with RPI (level = 36) model. The frame frequency was 120Hz, and the 1H time was 3.5 μs based on the FHD+ (1080 (horizontal) × RGB × 2280 (vertical)) resolution. All TFTs have a channel length of 3 μm. Fig. 2 shows the simulated I-V transfer curve of the LTPS TFT used in the proposed scan driver circuit. The V_{th} is set to -2.5 V.

4 Results and Discussion

Fig. 4 indicates the simulated voltage waveforms of Scan[n], Scan[n+1], and Sense[n] when the proposed circuit operated in the write period and blank period. We confirmed the stable outputs of Scan[n] and Scan[n+1] in the data addressing period and black data insertion period, respectively as shown in Fig. 4 (a). Fig. 4 (b) shows that Scan[n] and Sense[n] were fully discharged to VGL in the blank period. Thus, it was proved that the proposed circuit performs stable output operations.



(a)



(b)

Fig. 4 Simulation voltage waveforms of (a) Scan[n], Scan[n+1] in write period and (b) Scan[n], Sense[n] in blank period.

5 Conclusion

In this paper, we proposed a novel scan driver circuit based on LTPS TFT for black data insertion and external compensation method in the OLED display panel. The simulation results for the proposed circuit exhibit Scan[n] signal is stably pulled down to -5 V (VGL) during data addressing, black data. Likewise, Sense[n] is well output to VGL through SPGU during the external compensation period. In other words, the proposed circuit can realize the sense[n] output waveform to compensate for driving TFT of pixel circuit as well as scan[n] output waveform. Therefore, the proposed scan driver circuit can be adopted to the FHD+ resolution display panel.

References

[1] C.-L. Lin, W.-Y. Chang, C.-C. Hung, and C.-D. Tu, “LTPS-TFT pixel circuit to compensate for OLED luminance degradation in three-dimensional AMOLED display,” IEEE Electron Device Lett., vol. 33, no. 5, pp. 700-702, May. 2012.4

[2] Y.-H. Hong, E.-K. Jung, S. Hong, and Y.-S. Kim, “LTPS Technology for Improving the Uniformity of AMOLEDs,” SID Symp. Dig. Tech. Papers, vol. 52, no. 1, pp. 868-871, May. 2021.

[3] S.-K. Hong, B.-K. Kim, and Y.-M. Ha, “LTPS Technology for Improving the Uniformity of AMOLEDs,” SID Symp. Dig. Tech. Papers, vol. 38, no. 1, pp. 1366-1369, May. 2007.

[4] H.-J. In and O.-K. Kwon, “External compensation of nonuniform electrical characteristics of thin-film transistors and degradation of OLED devices in AMOLED displays,” IEEE Electron Device Lett., vol. 30, no. 4, pp. 377-379, Apr. 2009.

[5] J. Lee. J. Oh, E.-K. Jung, K.-C. Park, J.-H. Jeon, S.-Y. Lee, Y.-S. Kim, “High-reliability gate driver circuit to prevent ripple voltage,” J. Soc. Inf. Disp., vol. 29, no. 1, pp. 68-77, Jan. 2021.

[6] H.-J. Shin and S.-H. Choi, J.-Y. Choi, J.-K. Park, S.-H. Kim, S.-H. Yun, J.-R. Seo, S.-J. Bae, H.-S. Kim, C.-H. Oh, “A high image quality organic light-emitting diode display with motion blur reduction for ultrahigh resolution and premium TVs,” J. Soc. Inf. Disp., vol. 28, no. 6, pp. 557-565, Jan. 2020.

[7] J. Li, Y. Yuan, Y. Ding, W. Huang, Z. Ke, Y. Zhang, S. He, Q. Lai, and Y. Xu “Novel OLED Low Frame Frequency Driving Method with Minimized Flicker,” SID Symp. Dig. Tech. Papers, vol. 51, no. 1, pp. 680-682, May. 2020.