# LTPS Pixel Circuit with Leakage Current Compensating Mechanism for Smartwatch Displays

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**ABSTRACT**

*This work proposes a pixel circuit integrating a leakage current compensating mechanism. The pixel circuit suppresses the fluctuations of the driving current and eliminates the voltage variation at the gate node of the driving TFT by providing a compensation current. Therefore, the proposed pixel circuit is promising for smartwatch displays.*

## 1 Introduction

Active matrix organic light-emitting diode (AMOLED) displays are expected to become the mainstream of the next-generation displays thanks to their numerous advantages, such as fast response time, wide viewing angle, thinness, high brightness, and flexibility [1]. To date, among different manufacturing processes for pixel circuits of AMOLED displays, low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) are widely used because of their high mobility, outstanding driving capability, and small layout area [2], [3]. However, the non-identical threshold voltage ($V_{TH}$) of LTPS TFTs caused by the non-uniformity energy of excimer laser annealing (ELA) process leads to the OLED current variation under the same gray level, decreasing the image quality of displays [4], [5]. Hence, several pixel circuits have been developed to overcome $V_{TH}$ variations of LTPS TFTs for uniform OLED currents [6]-[9]. Lee *et al.* [7] proposed a pixel circuit composes of six TFTs and one capacitor to compensate for the $V_{TH}$ variations of the LTPS TFT and generates OLED current. Although this pixel circuit can compensate for the $V_{TH}$ variations of the LTPS TFT, the circuit produces a current flowing through the OLED during the programming period, decreasing the contrast ratio and bringing out the flicker phenomenon. Thus, the circuit generates extra power consumption and is undesirable for wearable applications. Accordingly, Kwon *et al.* [10] proposed a pixel circuit to solve the image flicker problem, increasing the image quality. This pixel circuit changes the voltage of the $V_{DD}$ signal during the compensation period to avoid the current flowing through the OLED. Although this pixel circuit can overcome the image flicker, it would produce additional power consumption because the frequency of charging and discharging the $V_{DD}$ signal line increases. However, power consumption is a critical issue for smartwatches that requires saving power consumption and extending life spans. To achieve low power consumption, the low-frame-rate driving method is widely used for the pixel circuit while adopting the low-frame-rate scheme prolongs the emission time. Nevertheless, the voltage stored at the gate node of the driving TFT is hard to be maintained during the prolonged emission time owing to the large leakage current of LTPS TFTs. Since the OLED current is determined by the source-to-gate voltage of the driving TFT, the distortion of the voltage at the gate node of the driving TFT caused by the large leakage current of the LTPS TFT severely influences the OLED current, resulting in poor image quality. Consequently, compensating for the $V_{TH}$ variations of the driving TFT and preventing the large leakage current of the LTPS TFT are required for a pixel circuit with the low-frame-rate method.

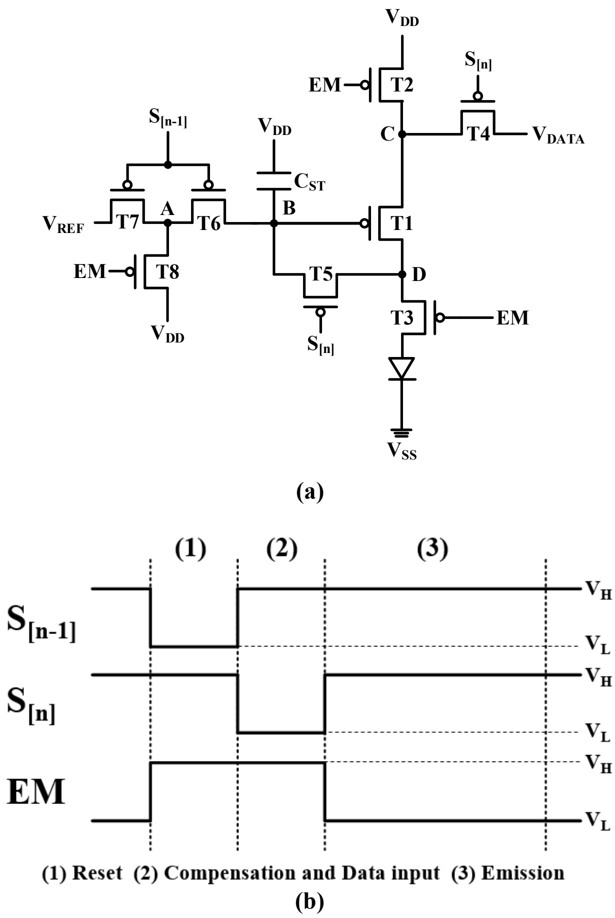


**Fig. 1 Proposed pixel circuit. (a) Schematic and (b) timing diagram of control signal.**

**Table I**
**PARAMETERS OF PROPOSED PIXEL CIRCUIT**

| TFT Aspect Ratio and Capacitance | | | |
|---|---|---|---|
| T1 (μm/μm) | 3 / 22 | T5 (μm/μm) | 3 / (3+3) |
| T2-T4, T6-T8 (μm/μm) | 3 / 3 | $C_{ST}$ (pF) | 0.4 |
| **Voltages of Signals** | | | |
| $S_{[n-1]}$, $S_{[n]}$ (V) | -4 ~ 5 | $V_{DD}$ (V) | 3.3 |
| EM (V) | -4 ~ 5 | $V_{SS}$ (V) | -3.3 |
| $V_{DATA}$ (V) | 2.5 ~ 3.3 | $V_{REF}$ (V) | -1.5 |

The proposed pixel circuit based on the LTPS TFT integrating a leakage current compensating mechanism ensures the voltage at the gate node of the driving TFT to be maintained during the prolonged emission time. In addition, the flicker phenomenon is eliminated by avoiding any current flowing through the OLED during the programming period. Simulation results indicate that the leakage current compensating mechanism absolves the variations of the voltage at the gate node of the driving TFT. Furthermore, the relative current error rates are suppressed below 4.5% as the $V_{TH}$ of the driving TFT varies by +0.5 V and -0.5 V, confirming that the proposed pixel circuit is prospective for the usage of the low-frame-rate smartwatch display.

## 2 Circuit Operation and Driving Scheme

Fig. 1 indicates the schematic and the timing diagram of the proposed pixel circuit. The proposed circuit is composed of one driving TFT (T1), seven switching TFTs (T2-T8), and one storing capacitor ($C_{ST}$). Notably, $C_{ST}$ is used to store the driving voltage of the pixel circuit. $V_{DD}$ and $V_{SS}$ are constant voltages. The operating principles of the proposed pixel circuit and the leakage current compensating mechanism can be divided into two parts, as described in the following.

### 2.1 Part A: Operating principles

2.1.1 Reset period

In the first period, $S_{[n-1]}$ goes low to turn on T6 and T7, so nodes A and B are discharged to $V_{REF}$ to reset the gate node of T1. EM goes high to turn off T2 and T3. Therefore, there is no current flowing through the OLED, enhancing the contrast ratio of the display.

2.1.2 Compensation and Data input period

During this period, $S_{[n-1]}$ goes high to turn off T6 and T7. $S_{[n]}$ goes from $V_H$ to $V_L$ to turn on T5. Node B is charged through the diode-connected structure of T1 until T1 is turned off. Therefore, the $V_{TH}$ of T1 and the data voltage are stored in $C_{ST}$. The voltage of node B can be written as follow:

$$V_B = V_{DATA} - |V_{TH\_T1}| \tag{1}$$

where $V_{TH\_T1}$ is the threshold voltage of T1.

2.1.3 Emission period

In the final stage, $S_{[n]}$ goes high to turn off T4 and T5. EM goes low to turn on T2, T3, and T8. The voltage of node A becomes $V_{DD}$, providing the compensating current for node B. The source node of T1, node C, becomes $V_{DD}$, while the voltage stored at the gate node of T1 is $V_{DATA} - |V_{TH\_T1}|$. Since the driving current is determined by the source-to-gate voltage of T1 the OLED current can be derived as follows:

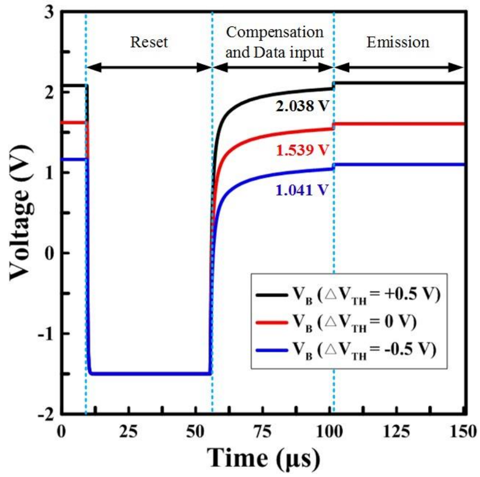


**Fig. 2 Transient voltage waveforms of node B with $V_{TH\_T1}$ variations of ±0.5 V.**

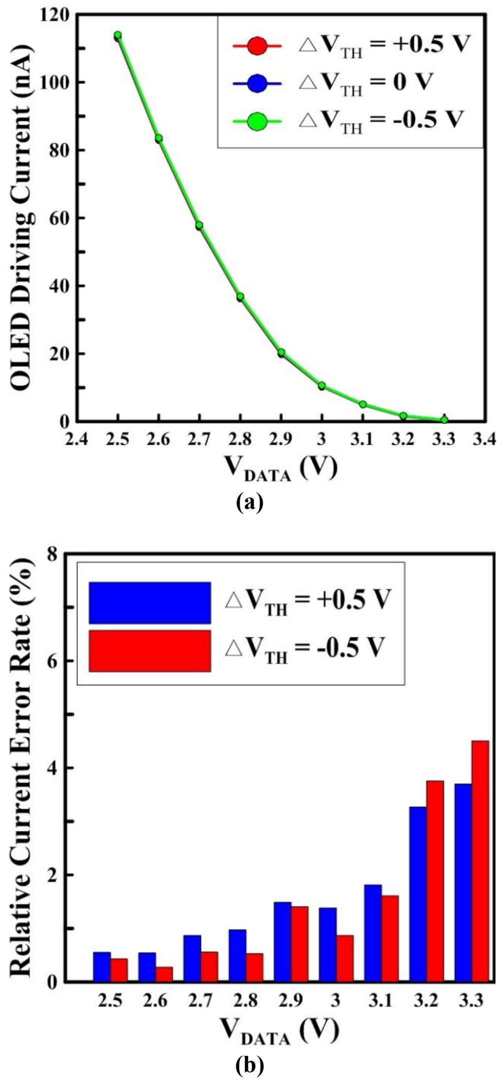


**Fig. 3 (a) OLED driving currents versus data voltage as $V_{TH}$ vary ±0.5 V. (b) Relative current error rates when $\Delta V_{TH}$ are ±0.5 V.**

$$
\begin{aligned}
I_{OLED} &= \frac{1}{2}k(V_{SG}-|V_{TH}|)^2 \\
&= \frac{1}{2}k\left(V_{DD}-V_{DATA}+|V_{TH\_T1}|-|V_{TH\_T1}|\right)^2 \\
&= \frac{1}{2}k(V_{DD}-V_{DATA})^2 \qquad (2)
\end{aligned}
$$

where k is $\mu \cdot C_{OX} \cdot W_{T1}/L_{T1}$. According to Eq. (2), the OLED current is independent of the threshold voltage of T1. Therefore, the proposed pixel circuit can compensate for the $V_{TH}$ variations of the driving TFT and generate stable OLED currents.

### 2.2 Part B: Leakage current compensating mechanism

The pixel circuit adopting the low-frame-rate method prolongs the emission time, so the voltage at the gate node of the driving TFT is easily affected by the leakage current of LTPS TFTs, causing fluctuations in OLED currents. Thus, the variations of the voltage at the gate node of the driving TFT caused by the leakage current of the LTPS TFT needs to be overcome. Hence, the proposed pixel circuit reveals a leakage current compensating mechanism to suppress the variations of the voltage at the gate node of the driving TFT. During the emission period, the voltage of node A becomes $V_{DD}$, utilizing T6 to provide the compensating current to balance the voltage drop at the gate node of the driving TFT. Consequently, the variations of the voltage of the driving TFT caused by the leakage current of LTPS TFTs during prolonged emission time is improved. Therefore, the proposed pixel circuit enhances the stability of the OLED current and is promising for low-frame-rate smartwatch displays.

## 3 Results and Discussions

To confirm the feasibility of the proposed pixel circuit, the HSPICE simulator with the RPI model (level = 62) is used to simulate the circuit for a 1.41-inch panel with the specifications of resolution of 320×360 and a frame rate of 15 Hz. Table I lists the circuit parameters including the aspect ratios of TFTs, the constant voltage of $V_{DD}$, $V_{SS}$, and $V_{REF}$, capacitance of capacitors, voltage swings of the control signals, and the data voltage range. Fig. 2 illustrates the simulated transient voltage waveforms of node B in the proposed pixel circuit when $V_{TH}$ of the driving TFT vary by +0.5 V and -0.5 V. The $V_{TH}$ variations of the driving TFT are accurately detected at the end of the compensation period to generate uniform OLED currents. Fig. 3(a) shows the simulation results of OLED currents versus data voltage with the $V_{TH}$ variations of ±0.5 V. After compensating for the $V_{TH}$ variations of the driving TFT, the circuit generates stable OLED currents without being affected by the $V_{TH}$ variations of the driving TFT. Fig. 3(b) shows that the relative current error rates of the OLED current when the data voltage range from 2.5 V to 3.3 V are all below 4.5%, verifying that the proposed circuit can generate uniform driving currents flowing through OLED devices. To confirm the effectiveness of the leakage current compensating mechanism of the proposed pixel circuit, the variations of the voltage at the gate node of the driving TFT of the proposed pixel circuit are compared with that of the conventional 4T2C pixel circuit [5], as shown in Fig. 4. Fig. 4(a) indicates the variations of the voltage at the gate node

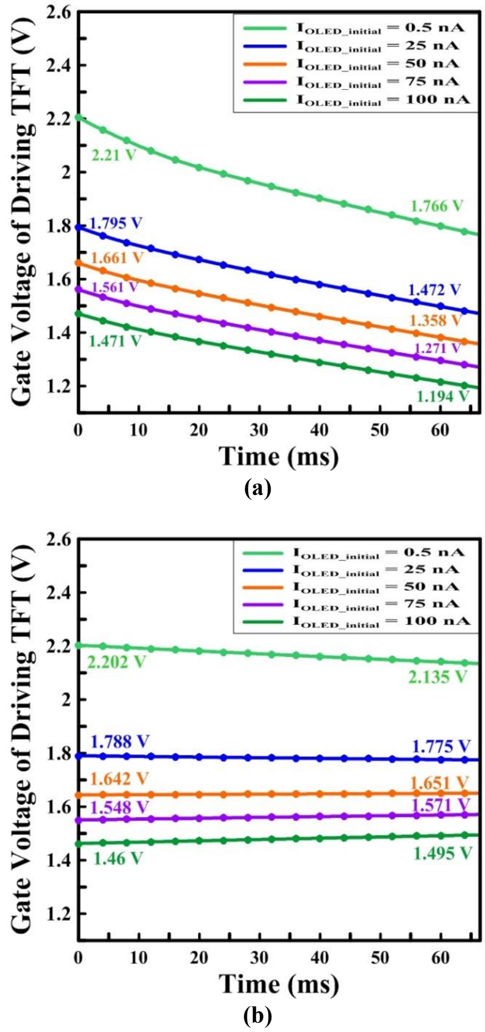


**Fig. 4 Variations of voltage at gate node of driving TFT of (a) 4T2C pixel circuit [5], and (b) proposed pixel circuit during emission period.**

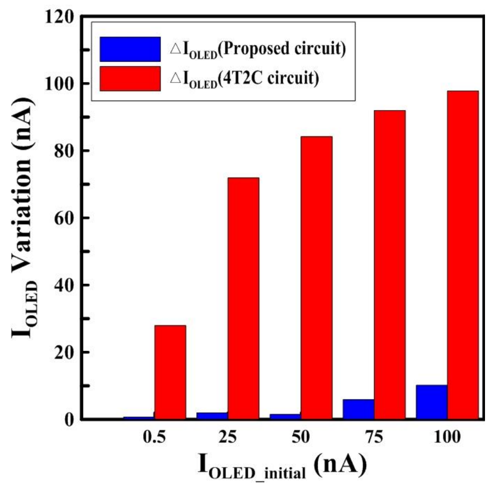


**Fig. 5 Comparisons of OLED current variations of proposed circuit and 4T2C pixel circuit [6].**

of the driving TFT of the 4T2C circuit during the prolonged emission time. When the initial currents are set to 0.5 nA, 25 nA, 50 nA, 75 nA, and 100 nA, the voltage of the gate node of the driving TFT varies 0.444 V, 0.323 V, 0.303 V, 0.290 V, and 0.277 V, respectively. Based on the simulation results, the voltage at the gate node of the driving TFT in the 4T2C pixel circuit is severely distorted due to the leakage current of LTPS TFTs. By contrast, the variations of the voltage at the gate node of the driving TFT of the proposed circuit are all below 0.067 V, as shown in Fig. 4(b), verifying the effectiveness of the leakage current compensating mechanism of the proposed pixel circuit. Fig. 5 shows the maximum variation of the OLED current of the 4T2C pixel circuit is 97.78 nA, while that of the proposed pixel circuit is 10.18 nA. The proposed pixel circuit with the leakage current compensating mechanism effectively suppresses the variation of the OLED current.

## 4 Conclusions

This work presents a pixel circuit integrating a leakage current compensating mechanism for use in smartwatches. According to the simulated results, the proposed pixel circuit shows that the relative current error rates are less than 4.5% when the $V_{TH}$ of the driving TFT varies by +0.5 V and -0.5 V. Moreover, the variations of the voltage at the gate node of the driving TFT are below 0.067 V, revealing that the proposed pixel circuit is highly suitable for use in smartwatch displays.

## 5 Acknowledgement

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