Device Model of Positive Bias Temperature Stress Instability for Oxide Semiconductor TFTs

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ABSTRACT

We propose a device model for oxide semiconductor thin-film transistors (OS TFTs) under positive bias temperature stress (PBTS). This model is a function of the channel interface electric field, and device simulations using this model reproduce measured PBTS degradation. The model is suitable for PBTS instability evaluation of OS TFTs.

1 Introduction

Oxide semiconductor thin-film transistors (OS TFTs) [1] show high field-effect mobility, a steep ON-OFF transition, quite low OFF current, and high stability (low sensitivity) under visible light conditions. These characteristics do not appear in conventional TFTs, such as hydrogenated amorphous Si (a-Si:H) TFTs, and originate from the electronic states and carrier transport properties of OSs. OS TFTs have been widely studied for novel display, sensor, and memory applications.

Electrical and temperature stresses often cause the OS TFT characteristics to degrade. The degradation is lower than that for a-Si:H TFTs, but can cause problems with operation of devices containing OS TFTs. There are several types of electrical and temperature stresses, including positive bias temperature stress (PBTS), negative bias temperature stress (NBTS), negative bias illumination stress (NBIS), and high drain voltage stress (HDVS).

In PBTS, a positive voltage is applied to the gate of the OS TFT and leads to a positive shift in the transfer curve [2-4]. The magnitude of the PBTS instability is evaluated based on the shift in the threshold voltage (V_{TH}). The V_{TH} shift is believed to be caused by electron trappings at and/or near the gate insulator-channel interface (GI-channel IF). A device simulation using the GI-channel IF trap reproduces the OS TFT characteristics after PBTS. This result supports the supposition above.

In contrast, electron trapping mechanism at the GI-channel IF is unclear. The shifts in V_{TH} with increasing stress time are usually represented by a stretched-exponential (SE) function. Because both conventional chemical reaction and Shockley-Read-Hall (SRH) trap-release models show exponential time dependences, they cannot explain the time dependence of the SE-type V_{TH} shift, which is shown in Fig. 1. Development of a device model to describe this time dependence would be helpful not only in understanding the mechanism of this shift, but also in investigations of device structures with high PBTS stability.

In this study, we consider a device model of the PBTS instability for OS TFTs. This device model is based mathematically on the SE model and includes two states at the GI-channel IF, an initial state, and a final state with electron trapping. The sum of the densities is determined using the bias voltage. The transition rate from the initial state to the final state is represented by a function of the GI-channel IF electric field, the value of which varies with PBTS time. A device simulation using this device model can reproduce the measured time variation in V_{TH} shifts [2] over a wide range of bias voltages and temperatures.

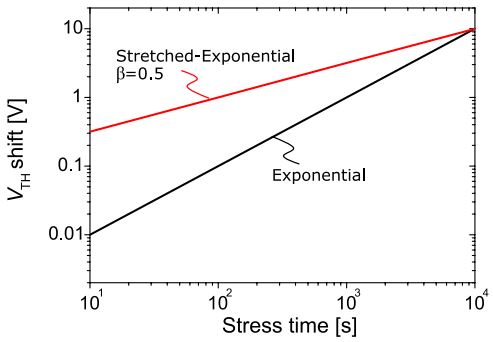

Fig. 1 Examples of shifts in V_{TH} with stretched-exponential and exponential time dependences

2 Device Model

The proposed device model is developed with reference to the formula for the SE function. In this model, there are two IF states ($S1$ and $S2$), and $S1$ changes into $S2$ via electron "e" trapping.

$$S1 + e- \rightarrow S2- , \quad (1)$$

where "$-$" expresses the negatively charged property. The state $S0$ represents the total IF state, and its density N_{S0} is equal to the sum of the densities of $S1$ and $S2$ (N_{S1} and N_{S2}):

$$N_{S0} = N_{S1} + N_{S2} . \quad (2)$$

The V_{TH} shift is given based on the SE model as

$$\Delta V_{TH} = \frac{qN_{S2}}{C_G} = \Delta V_0 \left\{1 - e^{-(t/\tau)^{\beta}}\right\}, \quad (3)$$

where q is the elementary charge, C_G is the gate insulator capacitance per unit area, t is the stress time, τ is the characteristic time, β is the SE exponent, and ΔV_0 is the V_{TH} shift after infinite stressing time. Based on the definition of $S0$, the relationship between N_{S0} and ΔV_0 is given by

$$N_{S0} = \frac{C_G\, \Delta V_0}{q}, \quad (4)$$

and the N_{S2} rate (dN_{S2}/dt) then becomes

$$\frac{dN_{S2}}{dt} = \frac{\beta}{\tau}\left[\ln\left(\frac{N_{S0}}{N_{S1}}\right)\right]^{-(1-\beta)/\beta} N_{S1}. \quad (5)$$

According to the Poisson equation and Gauss's law, the strong accumulation of the OS TFT under PBTS satisfies the following approximations [5]:

$$N_{S0} \sim \frac{\epsilon_S \left|\overrightarrow{F_{S0}}\right|}{q} \sim \frac{\sqrt{2\epsilon_S k_B T N_{es0}}}{q}, \quad (6)$$

and

$$N_{S1} \sim \frac{\epsilon_S \left|\overrightarrow{F_S}\right|}{q} \sim \frac{\sqrt{2\epsilon_S k_B T N_{es}}}{q}, \quad (7)$$

where ϵ_S is the OS permittivity, $\left|\overrightarrow{F_{S0}}\right|$ is the initial electric field magnitude at the GI-channel IF, k_B is the Boltzmann constant, T is the temperature, N_{es0} is the initial electron density at the GI-channel IF, N_{es} is the electron density at the channel IF at time t, and $\left|\overrightarrow{F_S}\right|$ is the electric field magnitude at the channel IF at time t.

The characteristic time for the SE model is given by

$$\tau = \tau_0 \exp\left(\frac{E_\tau}{k_B T}\right), \quad (8)$$

where τ_0 is the characteristic time constant, and E_τ is the activation energy. From an analogy with SRH theory, we can suppose a relation of

$$\frac{1}{\tau_0} = N_{S0} v_{thn} \sigma_n, \quad (9)$$

where σ_n is the electron trapping cross-length for the IF states (not the cross-section for bulk traps), and v_{thn} is the electron thermal velocity.

Substitution of Eqs. (6)−(9) into Eq. (5) leads to the following expression of the N_{S2} rate with respect to the IF electric field and IF electron density:

$$\frac{dN_{S2}}{dt} \sim \beta N_{S0} v_{thn} \sigma_n e^{-\frac{E_a}{k_B T}} \left[\ln\left(\frac{\left|\overrightarrow{F_{S0}}\right|}{\left|\overrightarrow{F_S}\right|}\right)\right]^{-\frac{1-\beta}{\beta}} C_r \sqrt{N_{es}}, \quad (10)$$

where C_r is the rate parameter, and E_a is the activation energy ($= E_\tau$). Note that when $\left|\overrightarrow{F_S}\right|$ is $\left|\overrightarrow{F_{S0}}\right|$ in the initial state of the PBTS, the right-hand side of Eq. (10) is equal to infinity. Therefore, this model assumes that $\left|\overrightarrow{F_{S0}}\right|/\left|\overrightarrow{F_S}\right|$ is 1.001 when $\left|\overrightarrow{F_S}\right|$ is equal to or more than $\left|\overrightarrow{F_{S0}}\right|$. In addition, we use the two proposed relationships for the parameters according to [2]. One is the temperature dependence of β, which is represented by

$$\beta = \frac{T}{T_0} - \beta_0, \quad (11)$$

where T_0 and β_0 are the constant parameters specifying the temperature dependence. The second is the expression for ΔV_0 given as

$$\Delta V_0 = C_v (V_{ST} - V_{TH0})^{\alpha}, \quad (12)$$

where C_v is the constant parameter, V_{ST} is the stress voltage applying to the gate electrode under PBTS conditions, V_{TH0} is the initial threshold voltage before PBTS, and α is the power factor.

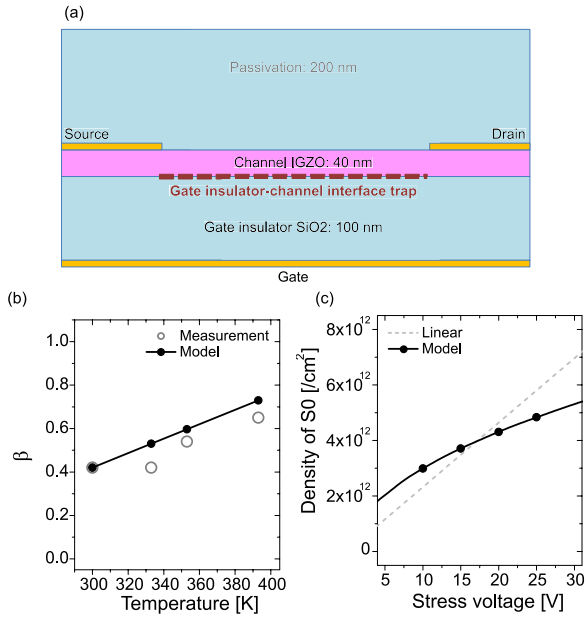

Fig. 2 (a) Diagram of simulated OS TFT structure; (b) temperature dependence of β (open circles: measured data; closed circles and line: this model); and (c) total IF state density (density of $S0$, N_{S0}) with respect to the stress voltage (gray dotted line: linear; open circles and line: this model)

3 Results

We investigated the possibility of use of this model via

device simulations (ATLAS, Silvaco Inc. [6]). Based on [2], the device structure and the model parameters are determined. Fig. 2 (a) shows a diagram of the simulated OS (amorphous In-Ga-Zn-O, a-IGZO) TFT structure, for which the channel and gate insulator thicknesses are the same as the corresponding values of the OS TFT in [2]. Fig. 2 (b) shows the dependence of β on temperature. The dependence in this model (i.e., closed circles and line) is comparable to the measured dependence (open circles). Fig. 2 (c) shows the total IF state density N_{S0} at each V_{ST} under PBTS (closed circles). The N_{S0} values at low V_{ST} are higher than those in the linear dependence case, where N_{S0} is calculated by Eq. (4) with $\Delta V_0 = V_{ST}$ (gray dotted line). Table 1 summarizes model parameters used in this study.

Table 1 Model parameters

Description [unit]	Symbol	Value
Gate capacitance (ε_r=4.2 for CVD-SiO_2) [F/cm^2]	C_G	3.72×10^{-8}
Electron capture cross-length [cm]	σ_n	7.9×10^{-25}
Electron effective mass (m_0 electron rest mass)	m_e	0.34 m_0
Rate parameter [cm$^{-1/2}$]	C_r	4.3×10^2
Activation energy of rate [eV]	E_a	0.77
Intrinsic temperature of β [K]	T_0	300
β intercept at T=0	β_0	0.58
Maximum voltage power factor	α	0.5
Maximum voltage constant parameter [V$^{-\alpha}$]	C_V	4.225
Initial threshold voltage [V]	V_{TH0}	0.7

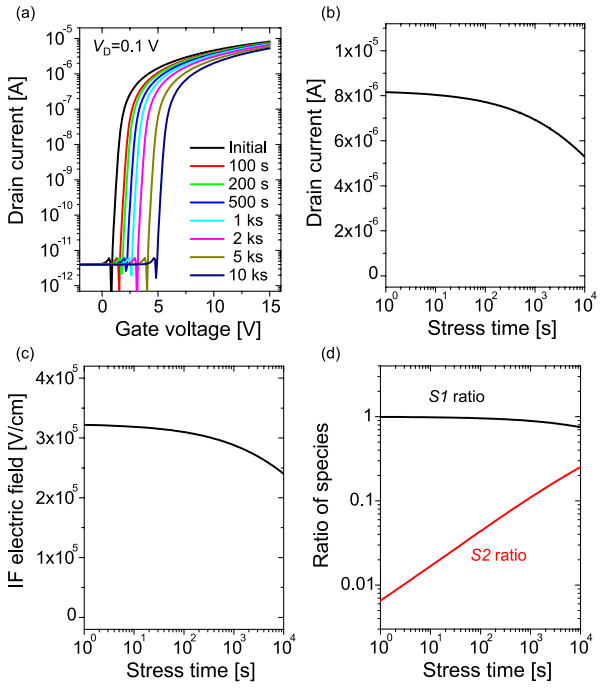

Fig. 3 Calculated properties of OS TFT under PBTS with V_{ST}=15 V and V_D=0.1 V at 300 K. (a) Transfer curves at V_D=0.1 V; (b) drain current versus stress time; (c) GI-channel IF electric field at the channel center; and (d) $S1$ and $S2$ ratios at the channel center (black line: $S1$ ratio; red line: $S2$ ratio)

We used this model to calculate the PBTS instability of the oxide TFT via the device simulator. Fig. 3 (a) shows the transfer curves at a drain voltage (V_D) of 0.1 V under 10 ks PBTS with V_{ST}=15 V and V_D=0.1 V at 300 K. These curves shift positively with increasing stress time. Under PBTS, the IF properties remain uniform along the channel because V_D is much lower than V_{ST}. The values at the channel center are, then, considered to be the common values. Figs. 3 (b) and (c) show the stress current and the channel IF electric field at the channel center, respectively, as functions of PBTS time. The IF electric field is shown to decrease with the decreasing current. The PBTS time dependences of the $S1$ and $S2$ ratios to $S0$ at the channel center are illustrated in Fig. 3 (d). The $S2$ ratio increases with an SE-like time dependence.

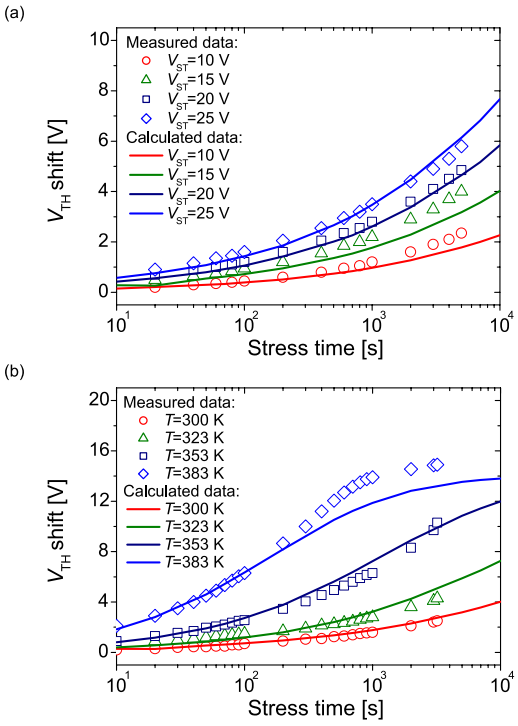

Fig. 4 (a) Shifts in V_{TH} under PBTS with V_{ST}=10, 15, 20, and 25 V at 300 K (symbols: measurements [2]; lines: calculations) and (b) shifts in V_{TH} under PBTS with V_{ST}=15 V and at temperature of 300, 323, 353, and 383 K (symbols: measurements [2]; lines: calculations)

Fig. 4 (a) shows the calculated V_{TH} shifts under PBTS with V_{ST}=10, 15, 20 and 25 V at 300 K (lines). As the figure shows, the calculated shifts are close to the measured shifts [2] (symbols). Fig. 4 (b) shows the calculated V_{TH} shifts under PBTS with V_G=15 V at 300,

323, 353, and 383 K (lines). The calculations reproduce the time dependence of the measured V_{TH} shifts (symbols) approximately at each temperature. These results indicate that the model can describe the PBTS instability of OS TFTs.

4 Discussion

Because the simulation using the device model can reproduce the PBTS instability, it is suitable for evaluation of the PBTS instability and its behavior in OS TFTs. In contrast, if the recovery from PBTS degradation [4] is to be considered, an additional model is required. The recovery usually takes a longer time than the degradation, and it can be accelerated by thermal treatment and light illumination. These characteristics indicate the possibility that holes play an important role in the recovery process.

Next, physical mechanisms of PBTS degradation are discussed. The SE behavior in this model originates from the exponential function of $\ln\left(\left|\overrightarrow{F_{S0}}\right|/\left|\vec{F}_S\right|\right)$ (or $\ln(N_{S0}/N_{S1})$) with the exponent factor of $-(1-\beta)/\beta$ in Eq. (10) (or Eq. (5)). We assume an electron capture model with phonon-assisted tunneling [7] and a reaction model acting via an intermediate state [8] as the physical mechanisms for this model. The references [3, 4] reported that the exponent factor β becomes approximately 0.5 without temperature dependence after post annealing for a sufficiently long time. This temperature-independent β is consistent with the physical mechanisms above. For example, according to the reaction model [8], the reaction rate to the final state via the intermediate state is proportional to the function $(N_{S0}/N_{S1}-1)^{-1}$. This function has the same form for the first order approximation of the Taylor series on $[\ln(N_{S0}/N_{S1})]^{-(1-\beta)/\beta}$ around N_{S0}/N_{S1}=1 when β is 0.5.

In contrast, the shallow tail state density of OS TFTs is much lower than that of a-Si:H TFTs [5]. Therefore, we believe that some models for a-Si:H TFTs (i.e., the hydrogen dispersion diffusion model [9] and the exponential barrier-distribution model [10]) are unsuitable for OS TFTs because the SE behavior in these models originates from the high tail state density of a-Si:H TFTs.

5 Conclusions

We proposed a device model for PBTS instability of OS TFTs based on the stretched-exponential model. The proposed model describes the transition from the initial state to the final state via electron trapping. The transition rate includes an exponential function of the logarithm of the interface electric field that decreases with increasing stress time. This function is the source of the stretched-exponential behavior.

The device model's viability was investigated via the comparison with measured device characteristics. Device simulations using this device model can reproduce the measured PBTS instability over wide bias and temperature ranges. This shows that the model is suitable for evaluation of PBTS instability of OS TFTs.

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