AMD6/AIS8-4L
(Late-News Paper)

5291-ppi OLED Display Enabled by Monolithic Integration of C-axis-aligned Crystalline IGZO FET and Si CMOS

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Keywords: CAAC-IGZO; OLED; Ultra high definition

ABSTRACT

For the first time in the world, we have fabricated OLED display that monolithically integrates Si CMOS, oxide semiconductor FETs, and OLED devices. The panel fabricated is a thin-bezel, > 5000 ppi OLED display with drivers embedded in the display area, enabling area savings of up to approximately 40%.

1 Introduction

Extended reality (XR), which has been garnering attention in recent years, takes various forms, such as augmented reality (AR), virtual reality (VR), and mixed reality (MR). Display panel for XR is different from that of a smartphone in that it requires extremely small form factors and extremely high pixel densities, fitting thousands of pixels per inch (ppi). To give an example in VR, unless the pixel density of the display is extremely high, the user will experience screen-door effects [1].

Si CMOS devices that are commonly used for high-pixel-density displays generally have excessive mobility for OLED current regulation. Hence, long-channel Si CMOS devices are used for lower current output. High-pixel-density displays with long-channel Si CMOS devices are difficult to achieve, one factor being that the long-channel Si CMOS devices do not easily fit into the smaller pixels [2].

Oxide semiconductor FETs (OSFETs) do not require such a long channel to regulate the OLED current, making them suitable for high-pixel-density displays. In fact, an OLED panel having over 5000 ppi has been enabled with OSFETs [3].

For XR displays, OLED panels are preferable over LCDs in terms of response times. Good motion display on OLED panels need the capability to duty drive. Therefore, XR requires not only high pixel densities, but also the extra transistors in the pixel to enable duty drive. There is no report on a > 5000 ppi high-pixel-density display that is capable of duty drive.

OSFET scaling for VLSI has advanced in recent years [4, 5]. OSFETs have higher breakdown voltage than Si CMOS devices [3], and thus are anticipated to enable high-pixel-density displays, even with complex pixel circuit configurations. The OSFET is also attracting attention as a back-end-of-line transistor that can be monolithically integrated with Si CMOS devices. Memory and normally-off CPU modules that exploit this and another feature of the OSFET, its extremely low off-state current [6], have been reported [7-10].

For this work, the source and scan drivers are fabricated with Si CMOS devices, and the pixels are monolithically fabricated with OSFETs using this VLSI technology. The panel has a pixel count of 1920 × 1920. If two panels are provided with one panel per eye, the total resolution becomes 3840 × 1920, providing an image comparable to a 4K panel. In addition, this panel's pixels are compatible with duty drive, achieving a smooth motion-image display. Because this panel has an extremely high pixel density (> 5000 ppi), the pixel is illuminated with white OLED device with a color filter (CF). Details are described in the following sections.

2 Si ＼ OS ＼ OEL Monolithic Structure and Characteristics of CAAC-IGZO FET

In this prototype, the source and scan drivers are fabricated with Si CMOS devices, and the pixels are fabricated with OSFETs directly over the drivers. Both processes are performed on one silicon wafer. Fig. 1 is a conceptual diagram of the Si＼OS＼OLED monolithic display.

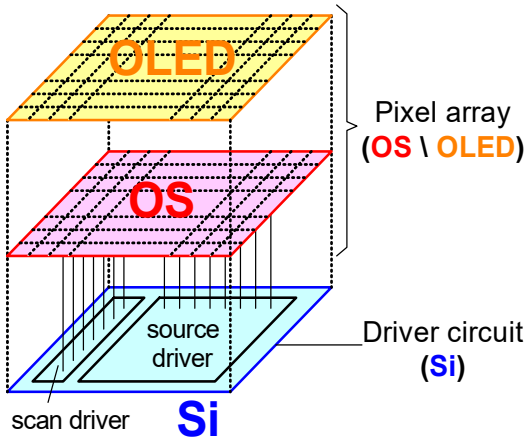

Fig. 1 Conceptual diagram of the Si＼OS＼OLED monolithic stack

Fig. 2 shows the process flow for the Si＼OS＼OLED display. The Si＼OS＼OLED display fabrication starts with Si CMOS devices and multiple metal layers on a Si wafer, using a process technology that is commonly used for display driver ICs on the market. Then, OSFETs and multiple metal layers are directly fabricated over the Si CMOS devices. After the OSFET fabrication steps, white OLED devices are evaporated, and CFs are placed to complete the OLED panel. As described, Si CMOS and OSFETs are monolithically integrated, and not fabricated on separate wafers and bonded together. This allows high-density interconnect between Si CMOS drivers and densely-packed pixels.

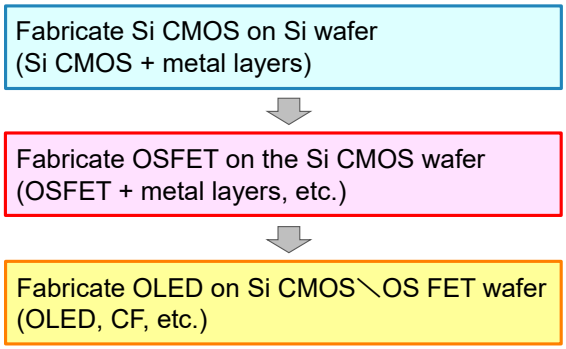

Fig. 2 Fabrication flow of the Si＼OS＼OLED monolithic stack

Fig. 3 shows the process flow of OSFET used for the panel of this work. After Si CMOS and multiple metal layers are fabricated, a base layer is deposited. The back gate electrodes are formed, then a back gate insulator, CAAC-IGZO as an OS material, and an S/D electrode materials are deposited. The film stack is patterned into islands, isolating the OS channels. Then, an interlayer dielectric film is deposited, and trenches are formed, simultaneously defining the S/D electrodes in a self-aligned manner. Then, a gate insulator and a gate metal are deposited. Subsequently, metal layers are deposited and patterned, and pixel electrodes and banks for OLED devices are formed.

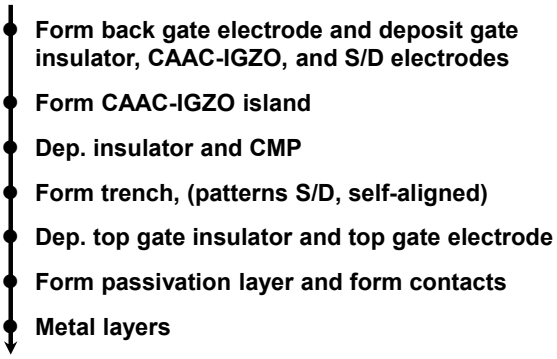

Fig. 3 OSFET Process flow

Fig. 4 shows the OSFET device structure. The FET is fabricated with a scaling-capable trench-gate-self-aligned (TGSA) structure [11] developed in the VLSI field, in which the gate electrode surrounds the channel, improving the gate electrostatic control.

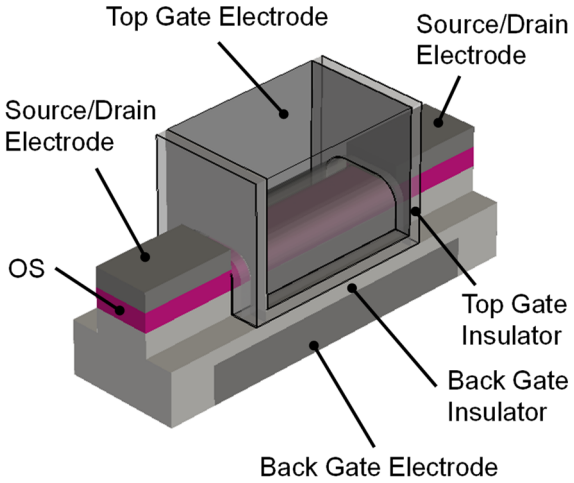

Fig. 4 Schematic view of OSFET (W/L = 60 nm/200 nm)

Fig. 5 shows the I_dV_g characteristics of an OSFET in a pixel of the prototyped display panel. Even with the scaled dimensions of the device (channel length: 200 nm, channel width: 60 nm, EOT: 10 nm), it is normally-off. In addition, the OSFET's off-state current is sufficiently low, below the lower measurement limit (1×10^{-12} A). Fig. 6 shows the OSFET I_dV_d characteristics. The scaled OSFET also exhibits good saturation.

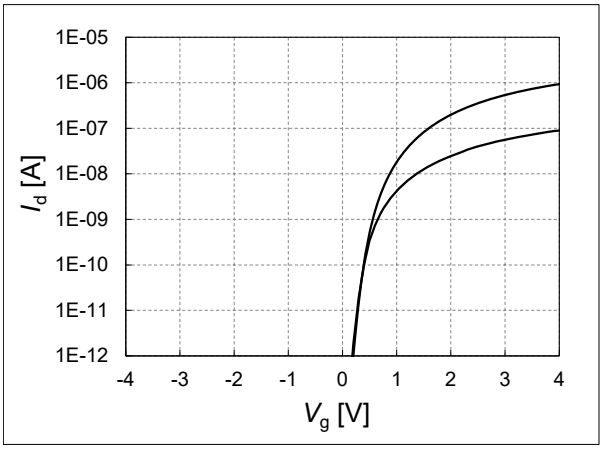

Fig. 5 Characteristics of OSFET (W/L = 60 nm/200 nm, V_{ds} = 0.1 V, 1.2 V)

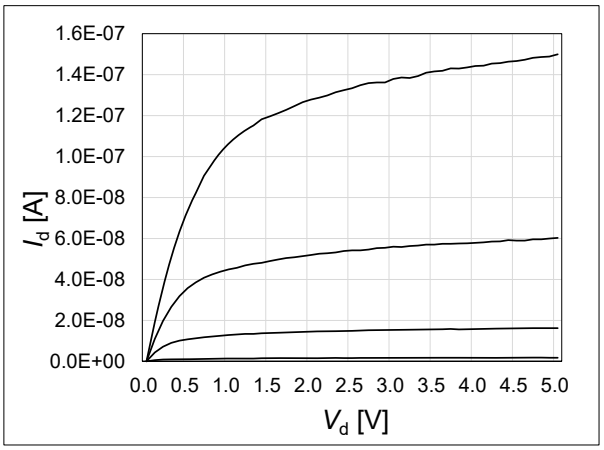

Fig. 6 Characteristics of OSFET
(W/L = 60 nm/200 nm, V_{gs} = 0.5V, 1 V, 1.5V, 2 V)

3 Pixel

3.1 Pixel Circuit

Fig. 7 shows the panel's pixel circuit, which is a 4T1C, duty-drive-compatible pixel, in which all transistors are OSFETs.

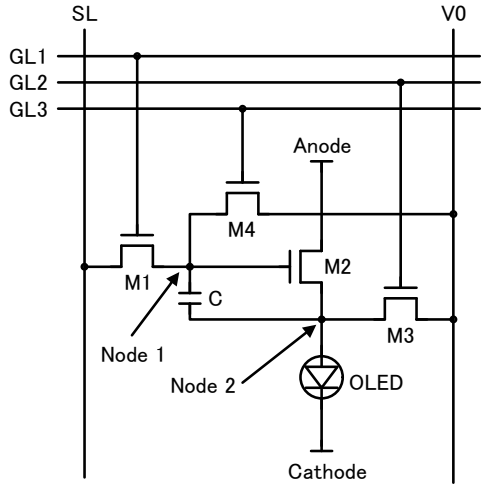

Fig. 7 Pixel circuit diagram

3.2 Pixel scheme

The panel operation is described using a timing chart in Fig. 8.

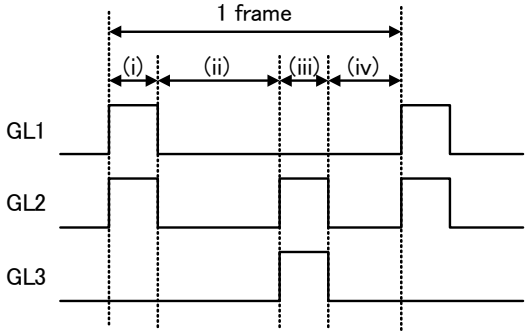

Fig. 8 Timing chart

(i) Write period: First, GL1 and GL2 are set high, and GL3 is set low. Data voltage V_{data} is written to Node 1 through SL, and a voltage V_0 is written to Node 2.

(ii) Light emission period: GL1, GL2 and GL3 are all set low, and the OLED device will emit light in reaction to a current from the drive transistor M2 that is determined by M2's V_{gs}.

(iii) Erase period: Then, GL1 is held low, and GL2 and GL3 are set high. At this time, the voltage V_0 will be supplied to both Nodes 1 and 2, which sets the V_{gs} of M2 at 0 V, turning off M2. This blocks the current supply to the OLED device, which stops emitting light.

(iv) Dark period: GL1, GL2 and GL3 are all set low, M2's V_{gs} is kept at 0V. The OLED device is kept dark.

Duty drive is enabled by changing the duration of period (ii), thereby changing the duration of OLED emission in one frame.

4 Driver circuits

Fig. 9 is the die photo of the panel in-prototype, before OSFET fabrication processes. Circuits such as source and scan drivers are fabricated in the display area with Si CMOS technology.

As such, Si＼OS＼OLED monolithic display would have a smaller chip area than a Si＼OLED display chip. Though it depends on the area for encapsulation and input terminals and other circuits in the chip, the Si＼OS＼OLED technology can save up to approximately 40% in area, enabling thin bezels not possible with pure-Si-CMOS backplanes.

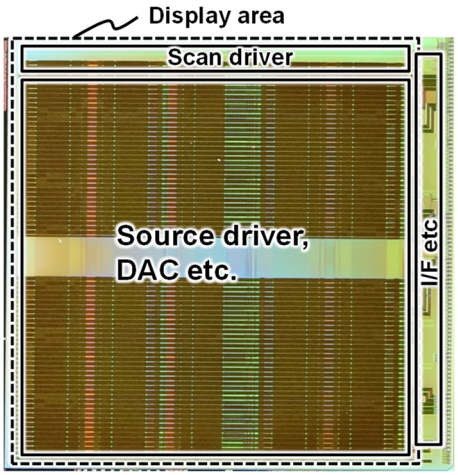

Fig. 9 Die photograph before OSFET fabrication

5 Results and Discussion

The panel fabricated for this work is described in Table 1.

Tandem devices are desired for reasonable efficiency in white OLEDs, but they require high voltages compared to single devices. Using tandem devices involves high voltages being applied to the pixel transistors, making OSFETs suitable for this application

as they have higher breakdown voltages than Si CMOS devices. The Si＼OS＼OLED monolithic stack is ideal in that it enables thin bezels by embedding drivers under the pixels, and utilizes the electrical advantages of both Si CMOS and OSFET devices appropriately.

Table 1 Panel Specification

	Specifications
Screen diagonal	0.51 inches
Resolution	1920 × 1920
Pixel size	4.8 μm × 4.8 μm
Pixel density	5291 ppi
Aperture ratio	23.8%
Coloring method	White Tandem OLED + CF
Emission type	Top emission
Source driver	Integrated (Si CMOS)
Scan driver	Integrated (Si CMOS)
Structure	Si＼OS＼OLED (monolithic)

Fig. 10 shows a photograph of the display panel prototype, demonstrating that both Si CMOS driver circuits and OS pixel circuits function properly in a monolithic integration to drive white tandem OLED devices. In addition, we have demonstrated the feasibility of duty drive.

Fig. 10 Picture of displayed image

6 Conclusion

We have, for the first time in the world, monolithically integrated Si CMOS and scaled OSFET devices and fabricated a thin-bezel, high-pixel-density (5291 ppi) OLED panel that is capable of duty drive and has white tandem OLED + CF.

In the Si＼OS＼OLED monolithic structure, a variety of non-display-driver Si CMOS circuitry can be placed below the pixels, in addition to the drivers. This can enable up to approximately 40% area savings and reduction in interconnects outside the panel. In addition, the pixels fabricated with the OSFETs can reduce its refresh rates [11, 12] to reduce power. They make the Si＼OS＼OLED technology suitable for versatile, low-power displays, making this technology a key enabler for next-generation AR/VR devices.

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