FLX4-4L
(Late-News Paper)

Low Voltage Operation of Organic Phototransistor Memory with Organic Charge Storage Layer

Reitaro Hattori[1], Takashi Nagase[1,2], Naoyuki Nishida[1], Takashi Kobayashi[1,2], Hiroyoshi Naito[1,2]

[1]Department of Physics and Electronics, Osaka Prefecture University, Sakai 599-8531, Japan
[2]The Research Institute for Molecular Electronic Devices (RIMED), Osaka Prefecture University, Sakai 599-8531, Japan

Keywords: Organic transistor memory, Solution-processable organic material, Organic charge storage layer

ABSTRACT

We report the low voltage operation of organic phototransistor memories with solution-processed organic charge storage layers by thinning the gate insulator. The organic memory devices with 140 nm-thick parylene gate insulators can achieve a high on/off current ratio of >10^3 with a programming voltage of 20 V.

1. INTRODUCTION

There has been considerable interest in the development of high-performance organic field-effect transistors (OFETs) for their potential usefulness in flexible and printed electronic devices [1]. Recent interest has also been directed towards the development of organic photodetectors [2,3] because of versatile demands for sensing devices in IoT society. Organic photodetectors have been combined with OFETs to fabricate large-area image sensor arrays [4]. Further, OFETs having photosensitive organic semiconductor films (organic phototransistors) have attracted growing interest to develop image sensors with a simple pixel configuration. Several researchers have reported the integration of a memory element in organic phototransistors to enhance photosensitivity [5], which can also facilitate large-area imaging by the simultaneous capture of the photogenerated signals on all the image pixels across the array [3].

In a previous study, we have developed a solution-processable OFET memory with a top-gate configuration by using the solution-processed blend film comprising a polymer insulator of poly(methylmethacrylate) (PMMA) and a soluble small-molecule semiconductor of 6,13-bis(triisopropylsilylenthynyl)pentacene (TIPS-PEN) as the charge storage layer [6]. The OFET memories based on poly(3-hexylthiophene) (P3HT) show large threshold voltage (V_{th}) shifts only when programmed under light illumination [7]. Such features can be applied to the solution processing of image sensor arrays with a memory function, which has been demonstrated using the P3HT FET memory [8]. Moreover, we have reported the improvement of the performance of OFET memories based on poly[2,5-bis(3-tetradecylthiophen-2-yl)thieno [3,2-b]thienophene] (PBTTT) by the addition of soluble fullerene derivatives to the charge storage layer [9].

In this study, we have examined the thinning of gate insulators and the application of drain voltage during programming and erasing processes in top-gate PBTTT FET memories with organic charge storage layers for low voltage operation. Consequently, programming and erasing voltage of the PBTTT memories could be reduced to sub-20 V, which is relatively lower than OFET memories using metal nanoparticles, etc. [10].

2. EXPERIMENTS

Figure 1 shows the device structure of a top-gate PBTTT FET memory and chemical structure of organic materials used in this study. The Au source and drain electrodes having thin Cr adhesion layers were defined on glass substrates by photolithography. After the surface of Au electrodes was modified with pentafluoro benzenethiol (PFBT) to form the hole injection layer, the organic semiconductor layer was fabricated by spin-coating a hot dichlorobenzene solution of PBTTT, followed by thermal annealing at 170 °C.

To fabricate the charge storage layer on the PBTTT film, PMMA, TIPS-PEN, and bis-phenyl-C_{61}-butyric acid methyl ester (Bis-PCBM) (weight ratio of 80:17:3) were

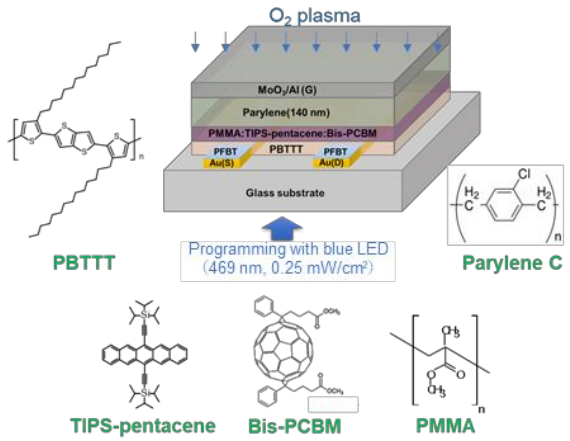

Fig. 1 Structure of a top-gate PBTTT FET memory with the PMMA:TIPS-PEN:Bis-PCBM (80:17:3) charge storage layer and chemical structure of organic materials used in this study.

dissolved in *n*-butyl acetate (an orthogonal solvent for PBTTT). This mixture was spin-coated on the PBTTT film, and the resulting thin film was annealed at 100 °C to enhance the vertical phase separation of TIPS-PEN and PMMA. After Parylene C was vacuum deposited to form the gate insulator with a thickness of ~140 nm on the charge storage layer, Al gate electrodes were fabricated by shadow mask evaporation. For comparison, we fabricated PBTTT FET memories with the ~300 nm-thick CYTOP gate insulator. The memory devices on the substrate were isolated by O_2 plasma etching with gate electrodes used as the etching masks. We also fabricated PBTTT FETs having a MoO_3 layer (5 nm) between the parylene gate insulator and the Al gate electrode to tune memory characteristics [11].

The preparation of organic films of memory devices and the measurement of memory characteristics were performed in glove boxes filled with N_2. A blue LED light (469 nm, 0.25 mW/cm^2) was exposed to the memory devices from the backside of glass substrates in the programming process.

3. RESULTS AND DISCUSSION

Figures 2(a) and (b) show the typical drain current (I_D)-gate voltage (V_G) (transfer) characteristics of PBTTT FET memories with Al gate electrodes having the parylene gate insulator (~140 nm) and the CYTOP gate insulator (~300 nm), respectively. Both memory devices exhibit V_{th} shifts to the positive V_G direction after programming with V_G = 20 V under blue LED light. The observed positive V_{th} shifts are caused by the photogeneration of electrons in the PBTTT layers and the subsequent storage of electrons into TIPS-pentacene molecules within the charge storage layers.

It can be seen in Fig. 2 that the use of thin gate insulators enables to increase V_{th} shifts to over 10 V as well as the improvement of transistor characteristics. The transfer characteristics of memory devices with thin parylene gate insulators show a smaller subthreshold

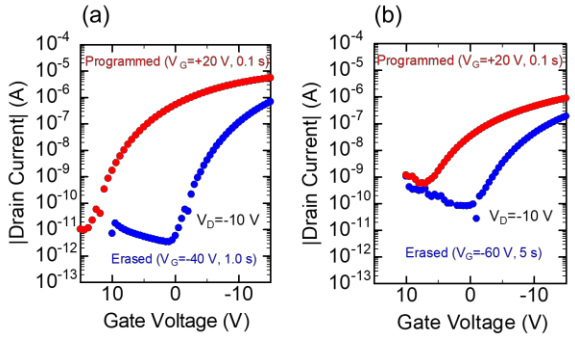

Fig. 2 (a) Transfer characteristics of PBTTT FET memory devices with 140 nm-thick parylene gate insulator and (b) 300 nm-thick CYTOP gate insulator measured after programming under blue LED light and erasing in the dark.

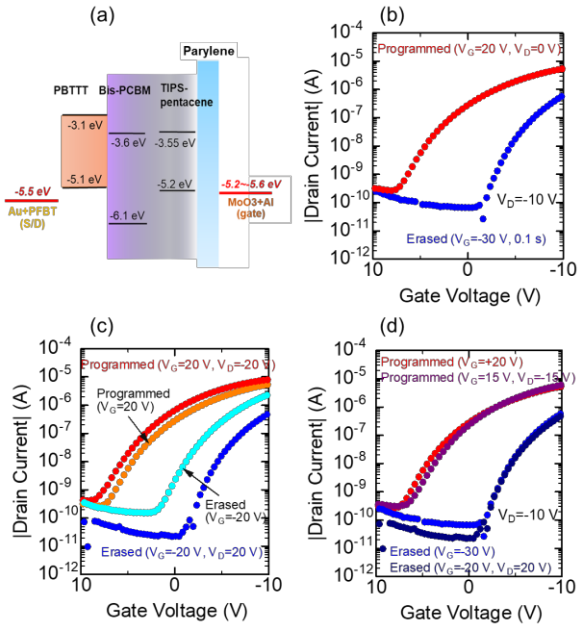

Fig. 3 (a) Energy band diagram and (b) transfer characteristics of PBTTT FET memory with the MoO_3/Al gate electrode. The programming and erasing voltages are V_G = 20 V and –30 V, respectively. (c) Transfer characteristics measured after programming (V_G = 20 V) / erasing (V_G = –20 V) with and without V_D, and (d) programming (V_G = 15 V) / erasing (V_G = –20 V) with V_D.

swing of 1.4 V/dec and achieve a higher I_D at V_G = 0 V even after programmed with V_G = 20 V. As a result, the ratio of I_D values at V_G = 0 V in the programmed and erased states is increased to over 10^3, which facilitates the readout process of stored photocarriers from memory devices.

As can be also seen in Fig. 2, PBTTT FET memory devices with the Al gate electrodes require the application of a high negative V_G of more than –40 V to erase the positively shifted V_{th}. Such behavior can be attributed to a large difference in the work functions of the Al gate electrode (–4.3 eV) and the PFBT-modified Au source-drain electrodes (–5.5 eV [12]), which likely causes a built-in potential and hence prevents the effective application of V_G in the erasing process.

To reduce the work function difference, a high work function metal oxide layer of MoO_3 (–5.2 ~5.6 eV) was inserted between the Al gate electrodes and the parylene gate insulator, as illustrated in Fig. 3(a). Figure 3(b) shows the transfer characteristics of PBTTT FET memory with the MoO_3/Al electrode and the PFBT-modified source-drain electrodes measured after programming and erasing processes. The memory device with the MoO_3/Al electrode enables erasing with V_G = –30 V, showing the effectiveness of the tuning of the work function of gate electrodes for reducing the erasing voltage of our memory devices.

The programming and erasing processes of OFET memories are generally performed with the source and drain electrodes set to 0 V [drain voltage (V_D) = 0 V]. It is found that the programming and erasing voltages of our memory devices can be further reduced by the application of V_D having the opposite polarity of V_G used for programming and erasing processes. Figure 3(c) shows the transfer characteristics of PBTTT FET memories programmed and erased with and without the application of V_D. We observe that the application of V_D during programming and erasing processes leads to the increase in V_{th} shifts, which is more pronounced in the erasing process. The memory devices exhibit complete erasing characteristics by the application of V_G = –20 V and V_D = 20 V. Figure 3(d) shows the transfer characteristics of the memory device when programmed with V_G = 15 V and V_D = –15 V and erased with V_G = –20 V and V_D = 20 V. Our OFET memory with the solution-processed charge storage layer demonstrated excellent memory operations with a high on/off current ratio of more than 10^3 using the relatively low programming and erasing voltages of approximately 20 V. Such operation voltages are much lower than those of conventional OFET memories with organic charge storage layers [10].

4. CONCLUSIONS

We have investigated the effect of thinning the gate insulator on the characteristics of top-gate PBTTT FET memories with the PMMA:TIPS-PEN:Bis-PCBM (80:17:3) charge storage layer. The use of thin parylene gate insulator (~140 nm) allows achieving a V_{th} shift of over 10 V and a high on/off drain current ratio of more than 10^3 even after programming with V_G = 20 V. We found that the erasing characteristics can be improved by tuning the difference in the work functions of the gate electrode and the source-drain electrodes using MoO_3 layers. It was demonstrated that the programming and erasing voltages can be further reduced by the application of V_D during programming and erasing processes.

ACKNOWLEDGEMENTS

This work was financially supported by Mitsubishi Foundation, by Murata Science Foundation, and by Iketani Science and Technology Foundation. It was partially supported by JSPS KAKENHI (Grant Nos. JP19H02599, JP20H02716, JP20K21007, and JP21H04564).

REFERENCES

[1] A. C. Arias, J. D. MacKenzie, I. McCulloch, J. Rivnay, and A. Salleo, “Materials and applications for large area electronics: solution-based approaches”, Chem. Rev. **110**, 3 (2010).

[2] K.-J. Baeg, M. Binda, D. Natali, M. Caironi, and Y.-Y. Noh, “Organic light detectors: photodiodes and phototransistors”, Adv. Mater. **25**, 4267 (2013).

[3] A. Pierre and A. C. Arias, “Solution-processed image sensors on flexible substrates”, Flex. Print. Electron. **1**, 043001 (2016).

[4] H. Kawaguchi, S. Iba, Y. Kato, T. Sekitani, T. Someya, and T. Sakurai, “A 3-D-stack organic sheet-type scanner with double-wordline and double-bitline structure”, IEEE Sensor J. **6**, 1209 (2006).

[5] Y. Chu, X. Wu, J. Lu, D. Liu, J. Du, G. Zhang, and J. Huang, “Photosensitive and flexible organic field-effect transistors based on interface trapping effect and their application in 2D imaging array”, Adv. Sci. **3**,1500435 (2016).

[6] F. Shiono, T. Nagase, T. Kobayashi, and H. Naito, “Organic floating-gate transistor memory based on solution-processed organic films”, Proc. Inter. Display Workshops **23**, 1440 (2016).

[7] F. Shiono, H. Abe, T. Nagase, T. Kobayashi, and H. Naito, “Optical memory characteristics of solution-processed organic transistors with self-organized organic floating gates for printable multi-level storage devices”, Org. Electron. **67**, 109 (2019).

[8] H. Abe, R. Hattori, T. Nagase, M. Higashinakaya, S. Tazuhara, F. Shiono, T. Kobayashi, and H. Naito, “Enhanced performance of solution-processable floating-gate organic phototransistor memory for organic image sensor applications”, Appl. Phys. Express **14**, 041007 (2021).

[9] R. Hattori, T. Nagase, M. Higashinakaya, S. Tazuhara, T. Kobayashi, and H. Naito, “Enhancement of optical memory characteristics of solution-processed organic transistor memories with polymer-small-molecule composite charge storage layers”, Proc. of Inter. Display Workshops **27**, 178 (2020).

[10] Z. Zhu, Y. Guo, and Y, Liu, “Application of organic field-effect transistors in memory”, Mater. Chem. Front. **4**, 2845 (2020).

[11] M. Higashinakaya, T. Nagase, H. Abe, R. Hattori, S. Tazuhara, T. Kobayashi, and H. Naito, “Electrically programmable multilevel nonvolatile memories based on solution-processed organic floating-gate transistors”, Appl. Phys. Lett. **118**, 103301 (2021).

[12] Y. Kuzumoto and M. Kitamura, “Work function of gold surfaces modified using substituted benzenethiols: Reaction time dependence and thermal stability”, Appl. Phys. Express **7**, 035701 (2014).