Analysis and Improvement on the Abnormal alignment At Au conduction points in Narrow border Product

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ABSTRACT

In this paper, it is found a high proportion of peripheral abnormal alignment during the picture quality test in narrow border products, showing ear mura, the corresponding pixel has dark lines, and the location is concentrated near the Au conduction points. Some ESD burns was found near the dark lines. The cause of ESD burns during Process has been analysised, and the mechanism has been studied, further-more, several improvement methods has been proposed..

1 Introduction

Thin film transistor liquid crystal display (TFT-LCD) is widely used in the display field, which benefits from its long service life, clear image quality and high reliability. With the increase of production capacity of each panel factory and the increasingly fierce market competition, it becomes particularly important to improve the competitiveness of products.

The picture quality test (T-sheet test) is the basic indicator of panel quality. Different customers will detect different images, and major panel manufacturers will set up t-sheet test in the factory after mod output, so as to stop defective products in time, that means higher quality performance on the client side.

2 Phenomena and cause analysis

2.1 Phenomenon description

In mod picture quality test, it is found that a high proportion of poor alignment is Occured, as shown in Figure 1. The poor performance is in local areas, showing ear shape, which only occurs on the source side.

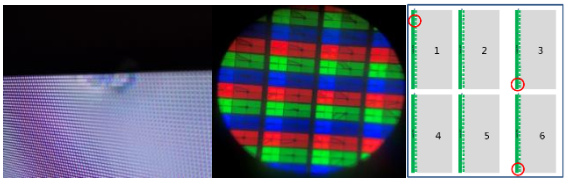


Fig. 1 Picture of abnormal alignment

2.2 Issue analysis

Through in-plane analysis, it is found that the defect is located at the Au conduction point, as shown in Figure 2, and there are obvious damage marks at the ITO via. Fig. 3a is the design diagram of the corresponding area. The injured part is adjacent to the metal line of Blue resist wall, and there is no abnormality at other conduction parts ;

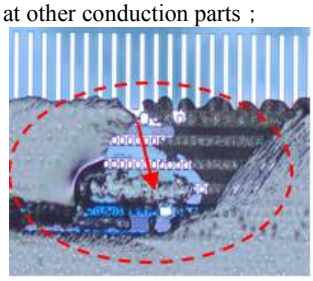
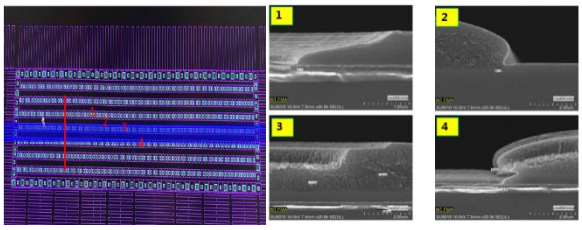


Fig.2 OM of Via hole Damage



a **b**

Fig.3 Location description and SEM of Damage area

Further SEM detection is carried out, and the detection position is shown in Fig. 3b. Position 1 is at the normal through hole of row 4, position 2 is at the edge of Blue resist wall , position 3 is at the through hole covered by Blue resist wall, and position 4 is at the junction between the lower edge of Blue resist wall and ITO Via hole. From the SEM results, it can be found that there is a slight undercut on the Blue resist wall at position 2 and the ITO at position 4 is disconnected, which is speculated to be the main cause of poor alignment ;

2.3 Cause analysis

Through further analysis of ITO disconnection, it is found that the dry process etches part of the PR that plays a protective role. With Blue resist in the Via area, due to PR is finally stripped, the dry etching rate does not affect the ITO connection. Then, With respect to those area with Blue resist Wall, there is a certain undercut in taper due to the Blue resist itself, and dry etching is slow due to complete crosslinking reaction of Blue resist , forming the chamfer of the Blue resist

wall, and ITO disconnection occurs In the subsequent ITO Sputtering Process.

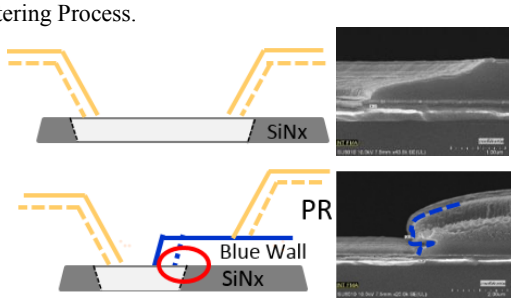


Fig.4 Illustration of Dry etching Process

2.4 ESD discharge path

Based on the analysis of the injury performance and the subsequent process involving voltage, it is speculated that the injury occurred at the HVA UVM site. The site needs voltage and UV light irradiation to make the reactive monomer in the liquid crystal material react and complete the liquid crystal alignment process. Due to the application of high voltage, the charge will be released according to the principles of conductivity, low voltage and proximity, The ITO disconnection leads to a large increase in resistance. At the same time, due to the undercut resistance of the color barrier wall, the charge is not easy to transfer quickly, resulting in charge accumulation and injury.

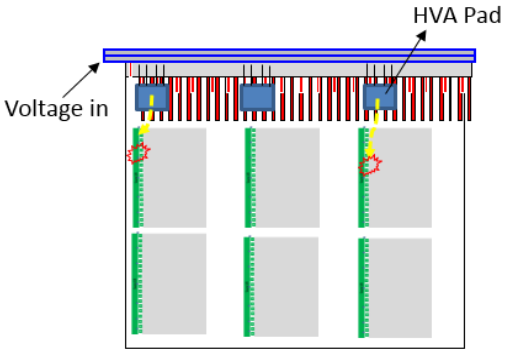


Fig.5 Abrigded general view of ESD discharge path

3 Improve Experiments and Results

3.1 Blue resistance taper improvement experiment

Through the process adjustment, the degree of crosslinking reaction was weakened to reduce the B taper, Detailed as, exposure energy decreased by 10mj and exposure gap increased by 50um. According to SEM, the taper of B at position 2 has been adjusted to the slope type without chamfer, but the undercut at the Via hole at position 4 still exists. Mod t-sheet test shows that the proportion of poor alignment has decreased, which proves that the Blue resist taper is one influencing factor of the ESD damage.

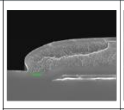
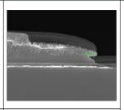
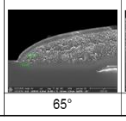
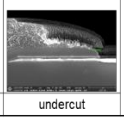
Blue Color resist	Align		SEM		Yield of Abnormal alignment (T-sheet)
	Energy /mj	Gap /um	Position 2	Position 4	
Standard condition	STD	STD	 undercut	 undercut	High proportion
Taper Improve contidion	STD-10	STD+50	 65°	 undercut	Low proportion

Fig.6 Results of Blue resistance taper improvement

3.2 different sensitivity experiment

In order to improve the undercut at the via, another B color resistance material with low sensitivity is selected for matching test. The sensitivity curves of the two color resistances are shown in Table 1 below. Under different exposure energy, the thickness change of the new color resistance film is 0.02 ~ 0.06um higher than that of the original B color resistance.

Table1 Variation of film thickness with exposure energy

exposure energy	Old B (um)	New B (um)
(25-20) mj	0.03	0.09
(30-25) mj	0.03	0.06
(35-30) mj	0.02	0.09
(40-35) mj	0.02	0.05
(50-40) mj	0.01	0.03

The T-sheet results show that the new B color resistance with low sensitivity has no poor alignment, which proves that dry etching rate is the main influencing factor of ESD. It is speculated that the color resistance material with low sensitivity is loose and easy to etch.

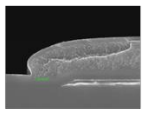
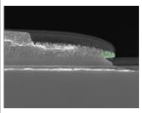
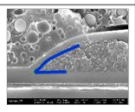
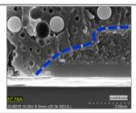
Blue Color resist	SEM		Yield of Abnormal alignment (T-sheet)
	Positon 2	Positon 4	
Old B	 undercut	 undercut	High proportion
New B	 37°	 OK	0%

Fig.7 SEM&T-sheet results of New Blue resistance

3.3 Improvement experiment of color resistance taper comprehensive voltage reduction

Based on the improved conditions of 3.1 taper, the HVA UVM process voltage is further reduced. The mod t-sheet test results show that the proportion of poor alignment is further

reduced, which proves that the HVA UVM voltage is also one of the influencing factors of ESD.

Table2 T-sheet results of different improved conditions

Item	Yield of Abnormal alignment (T-sheet)
Standard condition	High proportion
3.1 Taper *improvement* condition	Middle proportion
3.3 comprehensive condition	Low proportion

4 Conclusions

In conclusion, after confirming the phenomenon of poor alignment and corresponding analysis, we found that the cause of poor alignment is that the blue retaining wall set at the conduction point is chamfered due to etching, resulting in ITO disconnection at the conduction point. Under high HVA UVM voltage, local resistance is too high, resulting in electrostatic injury, resulting in abnormal alignment reduction, etc. There are three main factors causing electrostatic injury: Blue resist wall taper, dry etching rate and HVA UVM voltage, in which dry etching rate is the main factor. Since this is the first time to set the B photoresist on the via hole, it is necessary to take into account the film layer and film quality differences in the in-plane and peripheral areas. When it comes to the etching process, it is necessary to comprehensively adjust the front and rear process and film quality to find a balance, which is also a subject that needs to be continuously paid attention to and solved in the manufacture of LCD.

References

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