Improvement of MicroLED Efficiency Through Optimization of Electrode Area and Device Geometry

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Keywords: MicroLED, Efficiency, Emissive Displays,

ABSTRACT

MicroLEDs offer the potential to develop a variety of displays in a number of new formats and with exceptional performance with luminance, efficiency, and color gamut unavailable with other techniques. One of the challenges in microLED displays, however, has been the dramatic change in device efficiency over the bias applied in operating devices, especially as pixel size is reduced. In this work, we show a path towards optimizing the efficiency of small format microLEDs through optimization of the electrode area and reduction in damage to individual chiplets by reducing the area exposed to etching in microLED devices.

1 Introduction

Both microLED microdisplays and large area direct view displays have been using increasingly scaled LED pixels to achieve high resolution and low material use and cost.[1] The extraordinary luminance achievable using LEDs (20-50M nits+) reduces the requirements for LED fill factor, and at least in theory, allows for extremely small pixel elements; for many display formats these elements can be considered a the 1-10 micron scale.

In parallel with this demand for size scaling in LEDs, the relatively large (micron-scale) diffusion length in the GaN used in these devices also sets some limits for the practical minimum scaling possible for microLED chiplets (in mass transfer) and in patterned pixels (in monolithic microdisplays). Together with the increasing interest in sub-10 micron LED elements in microLEDs, it is worth considering the limitations for pixel scaling and practical approaches to overcome these challenges.

Many of the factors relating to microLED device scaling can be mapped to effects well known from large area LED device efficiency; namely recombination at chiplet sidewalls, optimization of current density, and damage due to etching in proximity of the recombination region. In this work we will discuss the strategies which can be considered for optimization of microLED efficiency and how structural optimizations can further enable the formation of miniature LED elements.

2 Mechanisms impacting efficiency

In all LEDs, it is well known that the efficiency is a sensitive function of the current density. This efficiency can be modelled using the A-B-C model2 and some measurements from our laboratory are shown below:

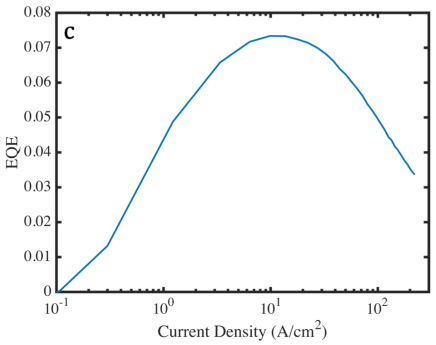

Figure 1: Current vs efficiency for an LED showing three regions of operation over varying current density – the optimum efficiency is seen at about 10A/cm2, both lower and higher current densities offer significantly lower efficiency.

Of greatest importance is the observation that there is an optimum current density for maximizing efficiency; this has both significant impact on microLED driving and indicates PWM drive; but also informs an important element in microLED structural design. Since there is an optimum current density for operation, there is necessarily also an optimum LED electrode area for each target luminance of a display; this area will, of course, also be different for each LED material.[3]

A second challenge is recombination at defects such as the surface of a chiplet. Chiplet-type devices require separation from the parent substrate, which leads to a certain introduction of some surface defects which have, so far, been challenging to passivate.

In microLED microdisplays, it is also common to define individual pixels using mesa etching. This isolation can provide a number of advantages; the mesa, cut into the high index LED material, waveguides the generated light out of the LED pixel, and some current confinement can also be achieved through the reduction in connectivity of the high conductivity layers in the LEDs. While the isolation offered can be strategic for many structures, it is well understood that the etched sidewalls also impacts the device efficiency when close to the LED active areas. It is clear that addressing and drive structures that permit

the configuration of electrodes without etched sidewalls approaching the LED layers, efficient devices can be fabricated with significantly smaller lateral dimensions.[4,5]

3 Strategies for improving scaled device efficiency

With these performance limitations in mind, there are several strategies that will be discussed in this presentation that have shown significant impact on microLED efficiency as devices are scaled.

3.1 Current density optimization

One of the more surprising conclusions in assessing the optimization of LEDs is the impact of mesa area on the overall system efficiency. Fig. 2, shows the current density and resulting efficiency.

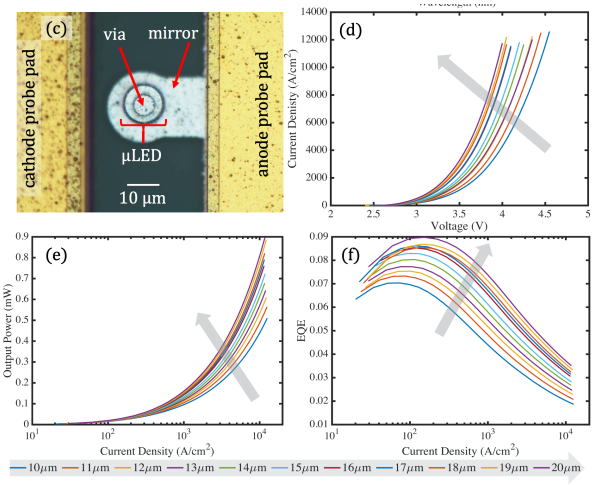

Fig. 2: Experimental results from reference 3, showing the difference in current density and resulting change in efficiency for mesas with a 10 micrometer diameter p-type contact and varying overall area under controlled bias conditions. Reproduced with permission under the terms of the OSA Open Access Publishing Agreement.

3.2 Sidewall current spreading reduction

In parallel with the optimization of LED electrode area, the current spreading observed leads to recombination at the LED etched mesa sidewalls. In parallel with optimization of the electrode and mesa area, organizing the electrodes to avoid injection of charge which can diffuse to defective surfaces offers an additional path for optimization of LED structures.

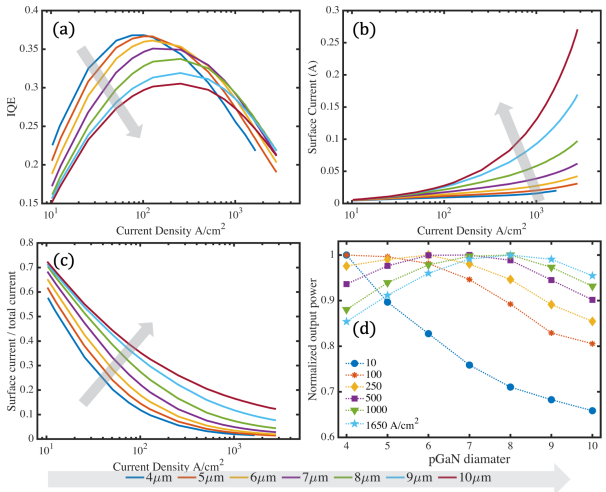

Fig. 3: Modeling results from reference 3, showing the difference in recombination/surface current for electrodes of varying size with a constant diameter mesa (10 microns). As the mesas approach the electrode size, even under the same current, the loss due to recombination significantly increases and exceeds half of the current under some conditions. Reproduced with permission under the terms of the OSA Open Access Publishing Agreement.

3.3 Sidewall etching elimination

While interruption of the crystalline lattice is unavoidable for chiplets, elimination of sidewall etching as a routine isolation technique for small LEDs is another option to consider for improving efficiency in small area LEDs. While such a configuration requires two-dimensional routing of the wiring (such as through use of a CMOS integrated circuit or thin film transistor addressing element), this approach can eliminate the need for etched pillar isolation, eliminating this source of inefficiency. Fig. 4 shows the constant efficiency seen when devices are isolated without sidewall etching.

Results for high efficiency small area LEDs will be presented using this technique.

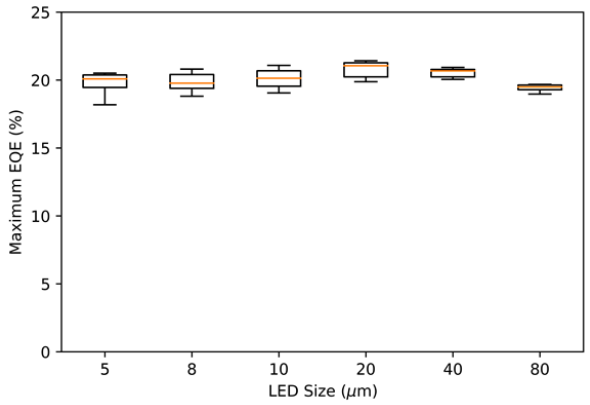

Fig. 4: Efficiency vs. size showing the independence of efficiency to LED size in the absence of LED etching.

4 Conclusions

MicroLEDs offer a number of systemic advantages over incumbent display technologies due to their extraordinary luminance, efficiency, and lifetime even at high current density. Despite outstanding overall characteristics, however, the same challenges seen in traditional LEDs also apply to microLED devices; namely significant variation in efficiency attributable to changes caused by changes in efficiency over varying current density and decreases in efficiency attributable to damage caused by etching in devices. In this work, we show that the efficiency and uniformity of microLED displays can be optimized through a strategic adjustment of the element isolation; namely optimization of the electrode size and avoidance, where possible, of etching for single device isolation.

Acknowledgements:
The authors appreciate the support of the National Science Foundation of the United States under program BCS:1926747, and the National Institute of Health under grant 1UF1NS116241-01.

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