Advanced Nano-scale Epitaxy for Full Color MicroLED Displays

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ABSTRACT

Nano-epitaxy shows great promise towards high quality LEDs on silicon wafers, which will be perfectly suited to micro-LEDs or micro-displays. In particular, the use of compliant nano-pillars is shown to reduce dislocation density and avoid strain in the layers.

1 Introduction

There is an ever increasing interest in micro LEDs and micro displays, in particular for virtual and augmented reality. Gallium nitride is well placed to respond to these applications, not only for blue and green LEDs but also with fast improving red emission. This is an important aspect, because AlInGaP based red LEDs have a severe reduction in external quantum efficiency (EQE) as pixels reach very small dimensions [1].

Currently, GaN based LEDs are grown on sapphire substrates, with a diameter of 100 or 150 mm. This limits their compatibility with the driver electronics which are typically available only on 300 mm diameter silicon. In this article we will describe an innovative approach using nano-scale epitaxy which paves the way towards high efficiency GaN devices on large silicon substrates.

2 LED epitaxy for micro-displays

GaN on silicon growth has two principal problems. The first is the difference in lattice parameter between GaN and silicon, which leads to the generation of dislocations. These have a negative impact on LED performance, at least until a level of around $1x10^{8}cm^{-2}$ is reached [2]. In order to resolve this problem, thick GaN layers are often necessary [3], which increases the cost and fragility of the wafers. The second problem for GaN on silicon growth is that there is a significant difference in the thermal expansion coefficient between these two materials, leading to a very large tensile strain in the GaN after growth, unless the layer stack is very carefully engineered. This requires that the GaN is grown under compressive strain that is imposed by previous AlN and AlGaN layers which have a smaller lattice parameter, as shown in Fig.1. This can be complicated to manage, in particular when the growth is performed on large diameter silicon wafers of 200 mm or more. As a result of these two problems, currently almost all blue and green LED production is therefore based on GaN on sapphire wafers, which are a more mature technology, with better quality GaN layers.

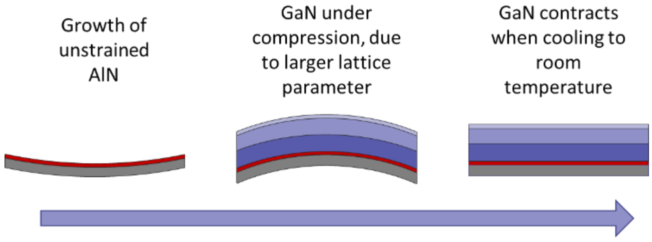

Fig. 1 GaN on silicon schematic

For improved micro-LEDs, and in particular for micro-displays, a bonding step can be applied between a silicon CMOS driver wafer and a light emitting GaN-based wafer [1] [4]. This allows the fabrication of devices with small light emitting pixels aligned to the driver wafer. Although sapphire wafers could be used for this process, they have a large convex bow imposed by the higher thermal expansion coefficient of sapphire, and a large Young's Modulus, making them hard to manipulate. Flat 200 mm wafers, with a low dislocation density and high performance emitters are therefore an important step towards higher quality and cheaper micro-displays.

3 Nano-epitaxial growth

A novel method for achieving these goals is shown in Fig.2. Initial thin AlN and GaN layers are grown on silicon on insulator (SOI) layers, before being patterned into nano-pillars. The growth then restarts as nano-pyramids, shown in Fig.3, before coalescing into small platelets, or vignettes [5]. Due to the compliance of the oxide layer within the nano-pillars at the growth temperature, the nano-pyramids are able to rotate when they join together. This allows them to align perfectly, reducing the elastic energy and also reducing the number of dislocations formed between neighboring pyramids. This is shown in Fig.4, where a transmission electron microscopy TEM cross-section image shows that for several of the coalescence boundaries (between each pair of pillars), there are no dislocations formed. This is not true for all of the coalescence boundaries, but this technique results in layers with a dislocation density of around $1x10^8 cm^{-2}$, the desired value for high quality LEDs.

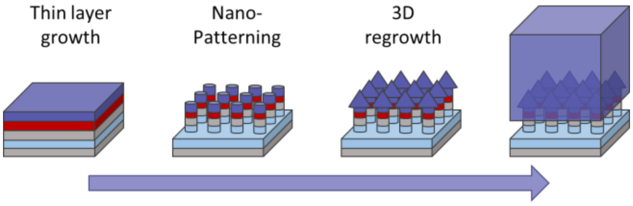

Fig. 2 Nano-epitaxy flow

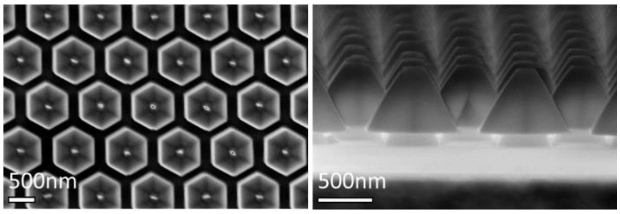

Fig. 3 SEM images of nano-pyramids

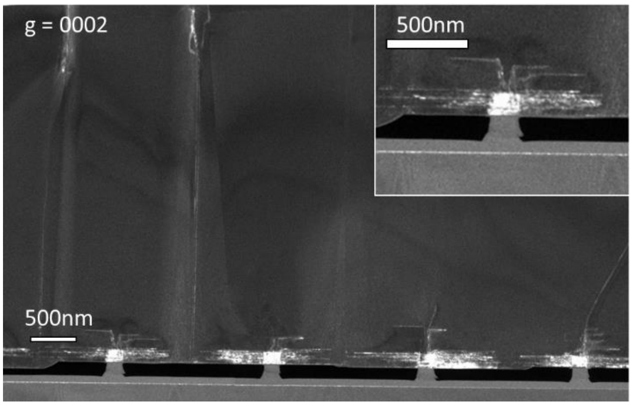

Fig. 4 TEM cross-section image of coalesced nano-pyramids, with zoom of broken nano-pillar (inset)

This technique then clearly enables the reduction of the dislocation density to the levels required for high quality LEDs, but it can also treat the problem of strain. In themselves, growth of GaN on silicon as small islands or mesas can reduce the strain and avoid cracking in the layers. However, the size of the mesa is limited and these structures tend to distribute the elastic strain in a non-uniform fashion, both laterally and vertically, with lower strain at the edges. It has previously been shown that different strain states affect the incorporation of indium into InGaN quantum wells and so the color of emission [6], which is not a desirable feature for well-defined color emission.

The use of nano-pillars is beneficial due to an important detail illustrated in the TEM image (inset Fig.4). Here we see that the nano-pillars are broken after growth and no longer connecting the GaN to the SOI wafer. The breaking of these pillars is likely to be due to the strain imposed during the cooling of the wafer from growth temperature. This disconnection allows the GaN layer to completely relax across the whole platelet, and so the problems of strain and strain uniformity on GaN on silicon can be overcome.

The rupture between the GaN and the substrate has an additional benefit in that it should avoid a significant bow being applied to the wafer, either during growth or when cooled to room temperature, ensuring easy wafer processing or bonding.

The platelets thus generated by the coalescence of nano-pyramids are shown in Fig.5 where we see a uniform and well-defined array, seen from above and in tilted view. There is little parasitic growth around them, and they are almost identical to one another. Previous studies have shown that by modifying the size of the localized growth structures, or by changing the spacing between them, it is possible to tune the color emission on different structures, even when they are all grown at the same time [7]. These results together show that appropriately dimensioned platelets formed from the coalescence of compliant nano-pillars should be capable of emitting across a wide range of colors, and would therefore be very well adapted for processing into pixels for micro-displays.

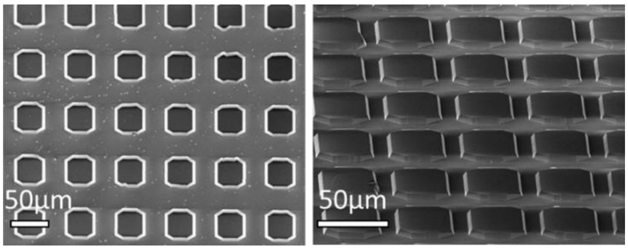

Fig. 5 SEM images of coalesced GaN platelets, from above (left) and with a tilted view (right)

4 Conclusions

Nano-epitaxy of GaN on silicon using silicon oxide as a compliant layer shows great promise for improved and cheaper full color micro-displays. The nano-pillars allow rotation of the different grains during coalescence, leading to low dislocation density in the resulting platelets. These platelets can be arranged in uniform arrays which are well adapted to the definition of pixels. In addition, during cool-down of the wafer, the nano-pillars under the platelets tend to break, thus ensuring strain free GaN at room temperature and avoiding the imposition of strain on the silicon wafers. This leads the way towards using 200 mm and even 300 mm silicon wafers as substrates for full color micro-display fabrication.

References

[1] Z. Chen, Yan, Shuke and C. Danesh, "MicroLED technologies and appliations: characterstics, fabrication, progress, and challenges," *J. Phys. D: Appl. Phys.,* vol. 54, p. 123001, 2021.

[2] S. Y. Karpov and Y. N. Makarov, "Dislocation effect on light emission efficiency in gallium nitride," *Applied Physics Letters,* vol. 81, p. 4721, 2002.

[3] K. Kim, "From the future Si technology perspective: Challenges and opportunities," *International Electron Devices Meeting,* p. 1.1.1, 2010.

[4] F. Templier, L. Benaïssa, B. Aventurier, C. Di Nardo, M. Charles, A. Daami, F. Henry and L. Dupré, "A novel process for Fabricating High-Resolution and Very Small Pixel-pitch GaN LED Microdisplays," *SID 2017 Digest,* p. 268, 2017.

[5] R. Dagher, P. de Mierry, B. Alloing, V. Brändli, M. Portail, B. Damilano, N. Mante, N. Bernier, P. Gergaud, M. Cottat, C. Gourgon, J. Zuniga Perez and G. Feuillet, "Pendeo-epitaxy of GaN on SOI nano-pillars: Freestanding and relaxed GaN platelets on silicon with a reduced dislocation density," *Journal of Crystal Growth,* vol. 526, p. 125235, 2019.

[6] A. Even, G. Laval, O. Ledoux, P. Ferret, D. Sotta, E. Guiot, F. Levy, I. Robin and A. Dussaigne, "Enhanced In incorporation in full InGaN heterostructure grown on relaxed InGaN pseudo-substrate," *Applied Physics Letters,* vol. 110, p. 262103, 2017.

[7] B. Damilano, M. Portail, E. Frayssinet, V. Brändli, F. Faure, C. Largeron, D. Cooper, G. Feuillet and D. Turover, "Blue to yellow emission from (Ga,In)/GaN quantum wells grown on pixelated silicon substrate," *Nature Scientific Reports,* vol. 10, p. p18919, 2020.