Nanoscale Patterning of Large-Area Electronic Devices at Low Cost

Gwenhivir S. Wyatt-Moon[1], Andrew J. Flewitt[1]

ajf@eng.cam.ac.uk
[1]Electrical Engineering Division, Engineering Department, Cambridge University,
9 J J Thomson Avenue, Cambridge CB3 0FA, UK
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ABSTRACT

Adhesion lithography is a technique which allows a controllable gap of length ~10 nm to be created between coplanar metal electrodes on a variety of substrates without the need for expensive, high-resolution patterning. This enables new levels of device performance for large-area electronics.

1 Introduction

The development of CMOS-based electronics over the last five decades has been built around reducing the minimum feature size in devices. This has enabled the development of high-performance microprocessors and high-density solid-state memories. The recent press release by IBM announcing a 2 nm chip technology is simply the latest incarnation of this trend [1].

However, the reduction in feature size has been accompanied by an increase in the cost of manufacture, not only in the capital equipment cost but also in running costs. For CMOS, however, the result can still be a viable business proposition as a large number of high value products can be manufactured simultaneously on each silicon wafer at high volume. The key metric here is actually the cost per device, which remains low.

Large-area electronics (LAE) is different. This is the branch of electronics where the main products have traditionally been displays and solar cells, but more recently other systems on 'unconventional substrates' like glass, plastic or even paper have been developed [2]. The recent publication of a thin film transistor-based machine learning processing engine by Ozer *et al.* is one example of this [3]. LAE would also benefit from following a CMOS-like trajectory of reducing feature sizes in devices, as this not only allows a higher density of devices, but in some ways even more importantly, an improvement in device performance, such as an increase in maximum frequency or a reduction in power. However, cost per unit area is the key metric for a viable business proposition in LAE rather than the cost per device for CMOS, and as a result the high cost and low speed per unit area of existing high resolution patterning techniques renders them unfeasible for LAE manufacturing and new approaches are needed.

2 Adhesion Lithography

2.1 Technique

Adhesion lithography has emerged in recent years a potentially transformative technique for patterning a well-defined gap of ~10 nm length between adjacent metal electrodes on a substrate [4]. The basic process is outlined in Fig. 1. A first metal is deposited and patterned on a substrate. A low-resolution process may be used for this step, such as direct printing of a metal ink and sintering, or a more traditional thin film deposition and photolithography process. The entire surface is then exposed to a solution of a long-chain organic molecule, such as octadecylphosphonic acid (ODPA) which is chosen to form a self-assembled monolayer (SAM) selectively on top of the first metal. The purpose of the SAM is to reduce the surface energy of the first metal such that when a second metal is patterned on the same substrate, again using a low-cost patterning process, the adhesion of the second metal to the first metal is significantly reduced compared with its adhesion directly to the substrate. Therefore, if a glue is applied to the substrate and peeled off, it will selectively remove the second metal only where it is over the first metal. The second metal fractures at the edge of the first metal and, depending on the fracture properties of the second metal, a well-defined nanogap of ~10 nm length is formed.

2.2 Tool

It is important that both the application of the glue and the subsequent peeling step is well-controlled in order to obtain both high yield and reproducibility. A simple

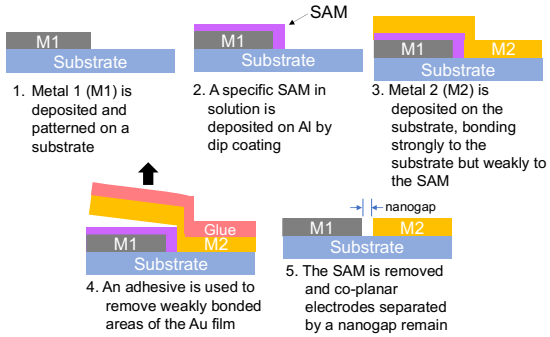

Fig.1 Schematic diagram of the adhesion lithography process.

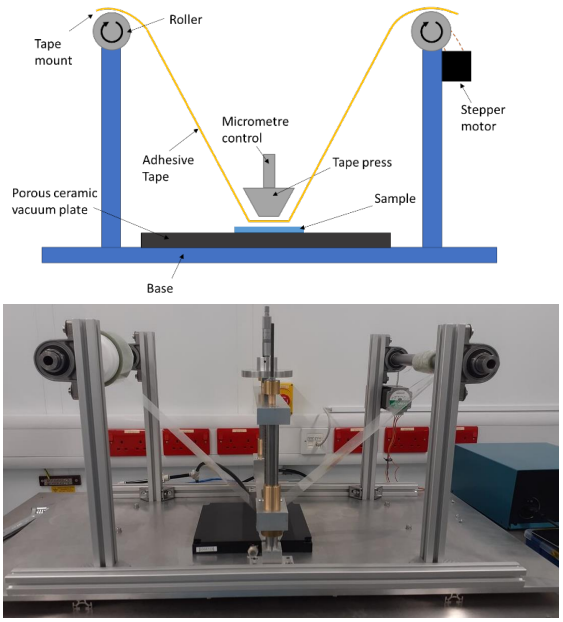

Fig.2 Schematic diagram (top) and photograph (bottom) of the adhesion lithography tool.

bench top tool has been developed to enable the adhesion lithography process to be executed on a variety of substrates up to 10×10 cm in size, although there is nothing that would intrinsically prevent scaling up to much larger substrate sizes. A schematic diagram and picture of the tool, detailed plans of which are also freely available [5], are shown in Fig. 2.

There are a number of features of the tool which are worthy of note. An adhesive-coated tape is used to achieve both the gluing and peeling steps. This means that the entire process is dry, which affords compatibility with substrates that would be degraded by contact with liquids, such as paper. The adhesive tape is mounted on a roller and fed underneath a tape press before being wound onto a second roller that is driven by an Arduino-controlled stepper motor which regulates the speed of the process. The substrate sits on a porous ceramic vacuum plate which simultaneously holds the substrate down onto the plate and allows lateral movement so that the adhesive tape can drag the substrate along as it moves. Finally, a tape press with a micrometer height adjustment allows a pressure to be applied to force the tape to temporarily adhere to the substrate. The tape press also precisely defines the angle of removal of the tape. The capital cost of the equipment is very low (<$11,000 for the system shown) as is that of the consumable adhesive tape. Therefore, the whole system is suited to the low cost per unit area structure of LAE.

2.3 Applications

Dissimilar materials can be used for the first and second metals, allowing asymmetric junctions to be formed. It is important that both metals strongly adhere to the substrate, that the side wall structure of both the first metal after initial patterning and the second metal after peeling are well defined, that the SAM adheres to the first metal and not to the substrate, and that the deposition and patterning of the second metal does not damage the SAM. Within these constraints, processes for using Al, Ni, Cr, Cu, Mo and Ti have been developed for the first metal, and Al, Ni, Cu, Cr and Au for the second metal.

A number of different thin film and nanomaterials have been successfully patterned into the nanogap to create Schottky diodes [6]. A key feature of these diodes is a very high cut-off frequency; this is a result of the coplanar electrode structure which means that parasitic capacitance is minimized.

3 Conclusions

Adhesion lithography provides a way of reliably patterning gaps between adjacent, dissimilar coplanar electrode with a length of ~10 nm. The capital cost of an adhesion lithography tool is ~100 times lower than traditional nanopatterning techniques such as e-beam lithography and the processing time is also much lower meaning that the cost structure is suited to large-area electronics.

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References

[1] "IBM Unveils World's First 2 Nanometer Chip Technology, Opening a New Frontier for Semiconductors." IBM. https://newsroom.ibm.com/2021-05-06-IBM-Unveils-Worlds-First-2-Nanometer-Chip-Technology,-Opening-a-New-Frontier-for-Semiconductors (accessed 2021/07/26, 2021).

[2] C. S. Buga and J. C. Viana, "A Review on Materials and Technologies for Organic Large-Area Electronics," (in English), *Adv. Mater. Technol.,* Review vol. 6, no. 6, p. 44, Jun 2021, Art no. 2001016, doi: 10.1002/admt.202001016.

[3] E. Ozer *et al.*, "A hardwired machine learning processing engine fabricated with submicron metal-oxide thin-film transistors on a flexible substrate," *Nat. Electron.,* vol. 3, no. 7, pp. 419-425, 2020/07/01 2020, doi: 10.1038/s41928-020-0437-5.

[4] D. J. Beesley *et al.*, "Sub-15-nm patterning of asymmetric metal electrodes and devices by adhesion lithography," (in English), *Nat. Commun.,* Article vol. 5, p. 9, May 2014, Art no. 3933, doi: 10.1038/ncomms4933.

[5] G. Wyatt-Moon and A. J. Flewitt. *Adhesion Lithography Peel Tool Design*, doi: 10.17863/CAM.68204.

[6] G. Wyatt-Moon, K. M. Niang, C. B. Rider, and A. J. Flewitt, "Air stable Indium-Gallium-Zinc-Oxide diodes with a 6.4 GHz extrinsic cut-off frequency fabricated using adhesion lithography," *IEEE Electron Device Letters,* vol. 41, no. 1, pp. 175-178, 2020, doi: 10.1109/LED.2019.2953982.