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New Structure of High Current Driving Oxide TFT for Ultra-High Resolution Display

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ABSTRACT

We introduce new structure of oxide TFT providing high current in a small footprint and suitable for the flexible display. Introduction of trench within the channel results in the thickness difference of semiconductors in the vertical and lateral regions. While the thicker lateral region of oxide semiconductor plays as a high current path, thin two vertical channels function as the semiconductors to yield acceptable V_{on} with boosting the current.

1. Introduction

Although the amorphous InGaZnO (IGZO) thin film transistor (TFT)[1]had been applied to the mass production of OLED TV, watch, notebook, and flexible display, there are still technical issues in adopting high mobility oxide TFT due to the channel shortening effect.[2,3] To implement the extended reality (XR), increase of pixel density is essential. As the mobility of oxide TFT increases, however, high mobility oxide TFT is vulnerable to have negatively shifted V_{on} by additionally added shallow donor such as hydrogen and oxygen vacancy. Therefore, it is very important to have well behaved high current driving oxide TFT within a small size to increase the pixel density.

When the channel width and length of high mobility oxide TFT are narrowed to decrease the allocated area, the drain current decreases in addition to the negative shift of the threshold voltage. To overcome these issues, we suggest trench structured oxide TFT which can boost the current flow in a small footprint as well as suppressing the negative V_{on} shift in spite of high current driving ability.

2. Experiment

To compare the electrical characteristics of the TFTs, two structures of planar (top gate staggered structure TFT[4] or self-aligned TFT[5]) and trench TFT were fabricated on the same substrate. All processes of the two devices were carried out simultaneously, except for the hole etching process for the trench formation. First, a 500 nm-thick SiO_2 buffer was thermally grown on a Si wafer. Next, trench holes with a depth of 200 nm were patterned on SiO_2. A 30 nm-thick high mobility oxide semiconductor, Al-ITZO, was deposited on SiO_2 as an active layer using the RF sputtering method at room temperature. After formation of source and drain (S/D) electrode of Mo, a 100 nm-thick layer of SiO_2 was deposited using PECVD as the gate insulator (GI). 150 nm-thick sputtered Mo was formed as the gate electrode. Subsequently, the samples were pre-annealed under vacuum at for 2 h. For the formation of self-aligned TFT, sequential patterning of the gate electrode and GI were carried out using the gate electrode. The active layer was exposed to Ar plasma treatment for 60 s at 100 W for the good contact with s/d electrode. Thereafter, the 100 nm-thick PECVD SiO_2 was deposited at 270 °C as an interlayer dielectric (ILD). A 150 nm-thick molybdenum S/D electrode material was deposited by sputtering method. Finally, a 10 nm-thick Al_2O_3 was deposited at 200 °C as a passivation layer. Active, gate, and passivation layers were patterned using a wet etching process. In contrast, SiO_2 buffer, GI, and ILD were patterned by a dry etching process. To compare the electrical performance of the planar and trench TFTs, they were annealed together under vacuum for 1 h after device fabrication.

3. Results and Discussion

Figure1 shows the structure of the planar and trench TFTs in a top gate top contact (TGTC), and figure 2 and 3 exhibit the electrical characteristics of each TFT after annealing at 230 °C.[4]

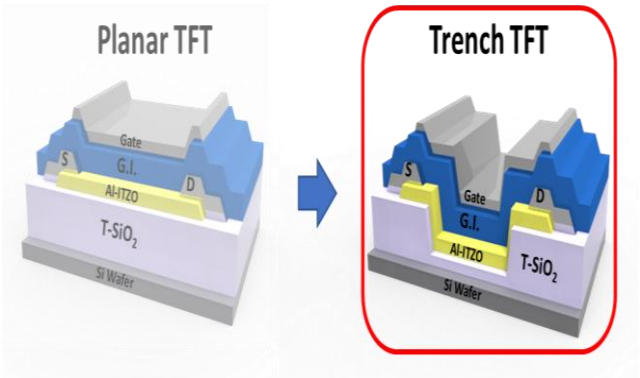

Fig. 1 Schematic diagram of Al- ITZO TFT in typical TGTC planar structure and with trench

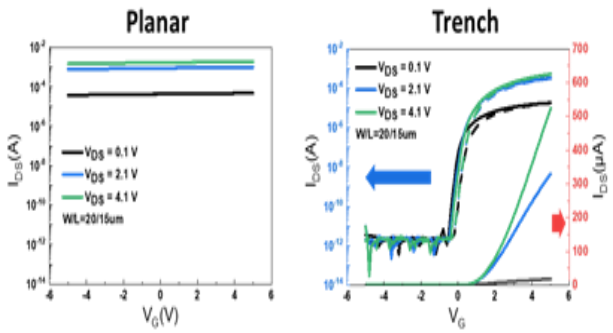

Fig. 2 Transfer curves of Al- ITZO TFT in typical planar structure and with trench after post annealing @ 230ºC

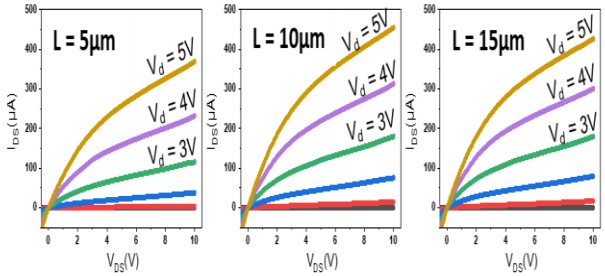

Fig. 3 Output curves of Al- ITZO TFT with trench depending on the channel length after post annealing @ 230ºC

While the TFTs in a planar structure became conductive after annealing, that with trench showed well behaved characteristics. However, the amount of electrical current from the trench TFT did not matched with the equation for the typical TFT. Rather, all trench TFTs showed relatively similar current level in spite of the different channel length. In other word, the mobility of the trench TFT increases or overestimated with increase of lateral channel length.

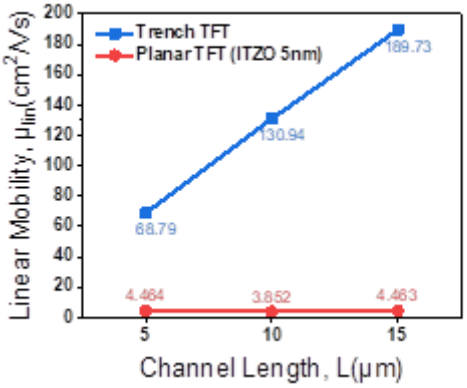

Fig. 4 Channel length dependence of each TFT

It is well known that the oxide semiconductor TFT has higher mobility with increasing carrier amount in the semiconductor. Therefore, the mobility of TFT would be increased with the increase of thickness and carrier concentration in the same film thickness. To investigate the origin of unique characteristics of trench TFT, we fabricated devices shown in figure 5. As the planar TFTs showed conductive behavior, device in figure 5 also exhibited conductive characteristics, indicating the conductive lateral region within the trench TFT, as does in the channel of planar TFT. From these results, we surmise while the horizon part of thicker Al-ITZO acts as fast current-path, the thin vertical semiconductors behave as effective channels. The TEM image of each part of trench are shown in figure 6.

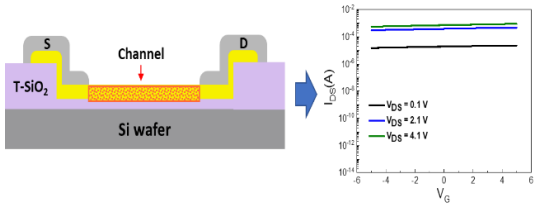

Fig. 5 I-V Characteristics of channel depending on the V_{ds}

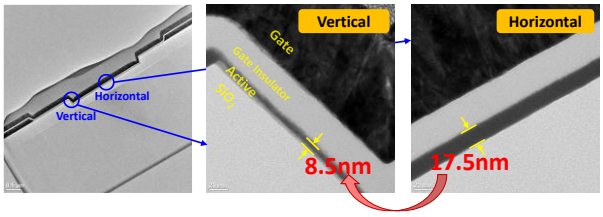

Fig. 6 TEM image of each part of trench TFT

Therefore, the insertion of trench within the active region yields two effective vertical channels as well as the planar fast current path.

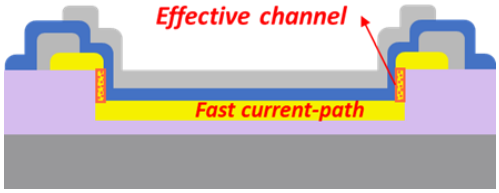

Fig. 7 Origin of high current in trench TFT

When we split the active thickness of TFT from 5nm to 30 nm, the planar TFT even with 5nm active layer resulted in well behaved TFT characteristics. Meanwhile, trench TFT with 5 nm of vertical channel showed just dielectric property. This implies that there are lots of scattering of carrier in the vertical regions of trench to hinder the current flow. We assume the rough vertical regions of trench, resulted from the lithography induce the scattering of carrier as identified by TEM analysis. This results in the reduction of mean free time of carrier and mobility to behave as effective channel within the

trench structure.

As well known, F in oxide semiconductor plays as a shallow donor. While the trench is formed within the SiO_2 film by means of dry etching using F based gas, F can be remained as residues on the surface of trench. For the planar TFTs, there was no difference between those with and without back passivation. The transfer curves of planar TGTC TFT yielded almost similar current. The trench TFT, however, yields decrease of current by the back-side passivation as shown in figure 7. This is because the F residues generated during the dry etching on the surface of trench play as the shallow donor to enhance the current amount.

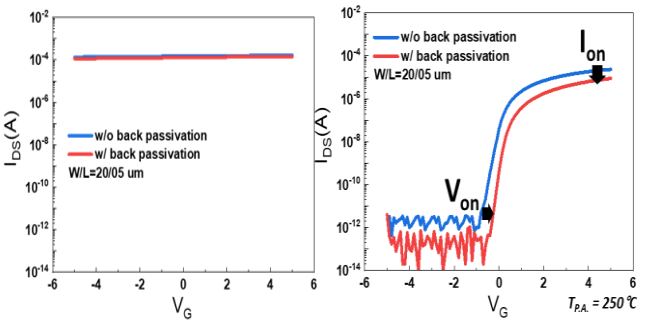

Fig.7 Effect of back passivation in planar and trench TFTs

For the ultra-high resolution display, making short channel TFT is very important with the reduction of RC delay. For the electrically stable short channel TFT, it is essential to suppress channel-shortening. Therefore, we introduced the trench within the self-aligned TFT to investigate the degree of channel shortening as shown in figure 8.

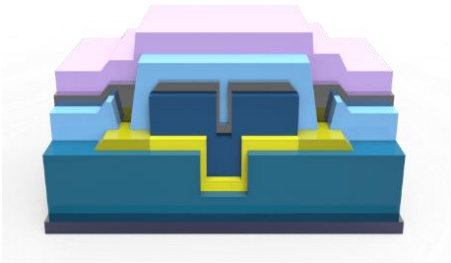

Fig. 8 Schematic diagram of Al-ITZO TFT in self-aligned structure with trench[5]

It is widely known that the newly generated and/or diffused H or oxygen vacancy (V_o) from the source/drain and passivation layer region toward the active region are the major origin of the channel shortening as shown in the figure 9. Oxygen vacancy can be easily generated by the reaction between the oxide semiconductor and metal. Therefore, selection of S/D material is very important to embody ultra-high resolution display. The trench oxide TFT can suppress the channel shortening regardless of source/drain material of the high mobility oxide TFT due to the high resistivity of oxide semiconductor in the vertical regions.

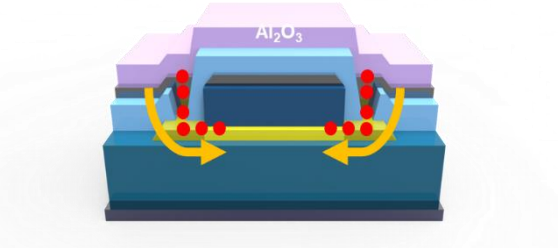

Fig. 9 Introduction of shallow donor into the channel to induce channel shortening in oxide TFT

In figure 10, the transfer characteristics of both SA Al-ITZO TFTs before annealing were almost identical and V_{ON} was 0 V with a hysteresis of 2.25 V. While the trench TFT exhibited on/off characteristics with V_{ON} of −1.25 V and hysteresis of 0 V, the planar TFT showed almost conductive behavior after annealing at 270 °C. The linear mobility of trench TFT with W/L= 20/10 increased up to 109 cm^2/Vs after annealing at 270 °C with stable switching characteristic. As the channel length increases, the mobility is overestimated.

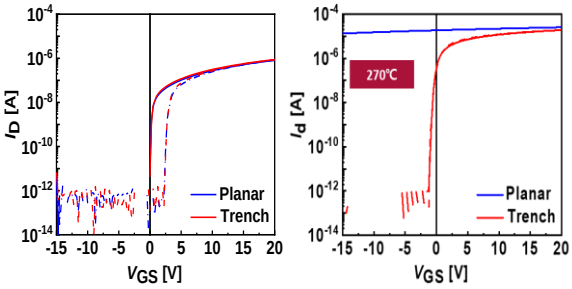

Fig. 10 Transfer curves of planar and trench TFT fabricated on the same substrate

Lastly, trench structured oxide TFT can have high stability in spite of rough back channel since higher thermal annealing can be possible with suppressing the negative Vth shift due to the high resistive vertical channel as shown in figure 11.

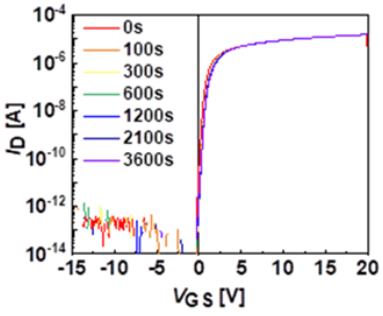

Fig. 11 PBTS of trench TFT under 1MV/cm at 60°C

4. Conclusion

Trench TFT provides high current in a small footprint to be suitable for the ultra-high resolution display. Vertical channels in the trench TFT has a higher resistance than the conductive horizontal channel because of the back-sidewall roughness and thin thickness. While the conductive lateral oxide film provides fast current flow, the resistive thin two vertical channels result in well behaved TFT with high on/off characteristics.

5. ACKNOWLEDGEMENT

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