Electro Static Discharge Optimization Based on Simulation

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Abstract

Electro Static Discharge (ESD), which occurs in the TFT-OLED process, leads the loss of display performance. In this paper, we establish a simulation model with which OLED design can be evaluated and optimized to avoid the ESD of the SD pattern process.

1. Introduction

Asymmetrical design of OLED metal wiring can cause many problems such as ESD, film uniformity, low utilization space, yield loss etc. Especially, in the process of TFT production, the electrostatic Breakdown issue seriously affects the yield of TFT (figure 1).With simulation (figure 6), we find that, the higher the SD pattern density is, the higher the electrostatic voltage between adjacent metal wires is. So the layout of metal wire needs to be optimized. In order to evaluate and optimize the panel design, we establish a simulation model with Ansys software. Several factors such as the position where electrostatic damage occurs easily, the transmission path of electrostatic charge, the position of a large electrostatic charge stayed, are taken into account in order to establish the ESD model.

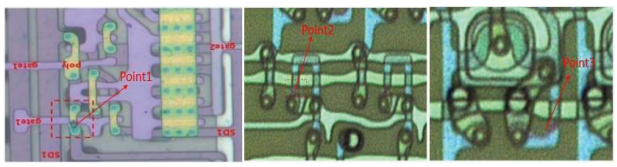

Figure 1. ESD damage location of Poly-Si

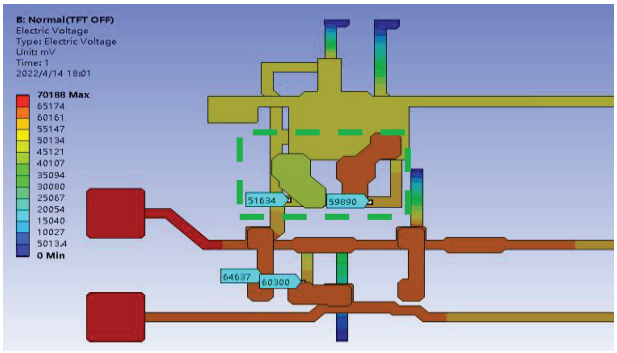

Figure 2. Simulation of electrostatic transmission path

2. Simulation Logic

2.1 Factors of ESD damage

In this paper, all the electrical simulation is based on composite metal films. The simulated parameters include film thickness and thermoelectric properties of materials. Figure 2 is the electrostatic charge transmission path simulation result. It can be seen that when large electrostatic voltage is applied on the left SD pattern, electrostatic charge is exported to the other four paths which is marked blue in Figure 2. The voltage distribution diagram shows its voltage transmission path, and we can see that the position where ESD damaged occurs has a high voltage. This simulation result matches the reality, which can be seen in figure1.

2.2 Occurrence mechanism

Figure 3 shows how the ESD occurs. It is divided into three stages, including electrostatic accumulation, capacity coupling and electrostatic charge transmission.

When EUV light hits SD pattern, photoelectric effect occurs. SD loses electrons and becomes positively charged, electrons as released into the air above the pattern. At the same time, free charge which accumulated from previous process is also collected on the SD surface due to the antenna effect. As a result, the EUV tube and SD pattern form a capacitor. As the electric potential difference becomes larger, the air between EUV and SD pattern is easily broken down and becomes a conductor. This makes the charged EUV tube and SD pattern form a circuit pathway and a lot of electrostatic charge transmits to SD pattern. As a result, the poly-Si is broken down.

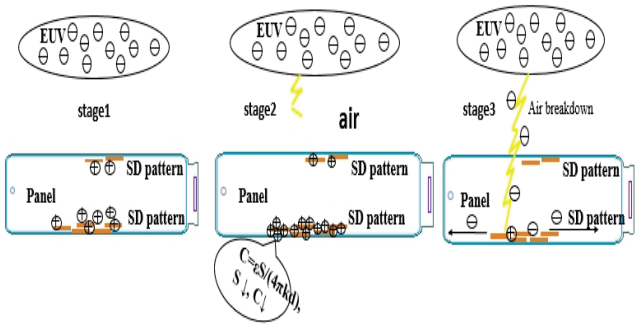

Figure 3. Electrostatic mechanism: electrostatic induction, dynamic transmission, electrostatic charge transmission

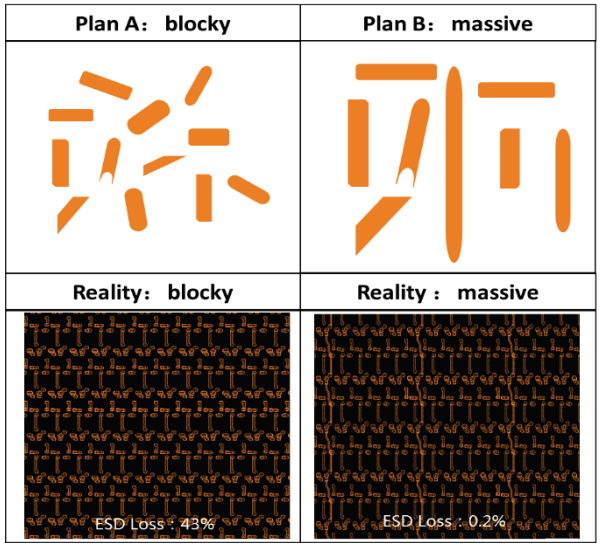

Figure 4. Different SD wiring methods leads to different ESD Loss

This can be explained by Capacitance formula: $C=\xi^{*}S/4\pi k^{*}d$ [1]. In this formula, ξ means a natural constant, S means the opposite area of the capacitor plate, k means the electrostatic constant, d means the distance between capacitor plates. With the same d, the smaller the S is, the smaller the C is. When the electrical charge is too much to be hold by the capacitance, the air between the SD pattern and the EUV tube can easily be broken down and become a conductor. That's why ESD occurs more easily when SD structure changed into blocky. In figure 4, Plan A means blocky, Plan B means massive, the yield loss of plan A design is 43%, and the loss of plan B is 0.2%.

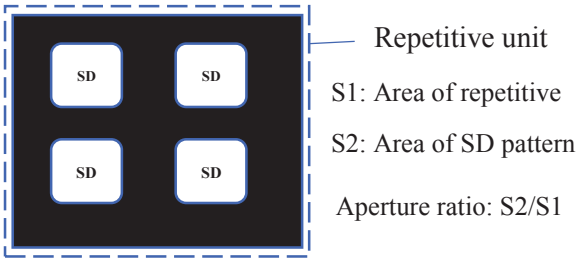

Figure 5. Electrostatic field intensity simulation of different SD density

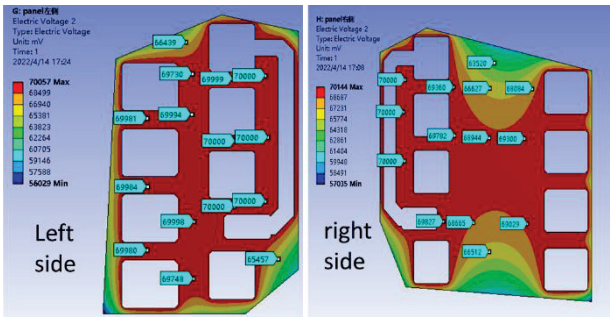

Figure 6. Electrostatic field intensity simulation of different SD density

2.3 Influencing factors of SD pattern aperture ratio

Generally, electrostatic damage occurs in the area with high metal wire aperture ratio. With simulation, we find that the SD pattern aperture ratio (figure 5) make influence on the electric potential. The higher the aperture ratio is,

the higher the electric potential is (figure 6), and the more the electrostatic charge is. Because metal wiring is asymmetrical, ESD electric damage occurs on the denser wiring side easily. As a result, ESD tends to occur on the left side.

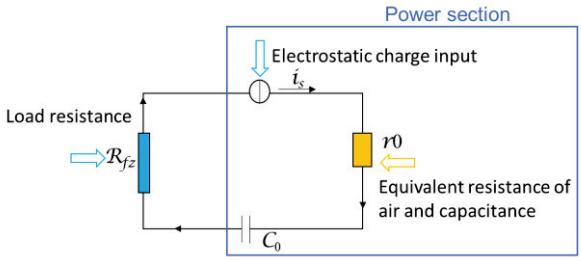

Figure 7. Equivalent electric circuit diagrams

Table 1. Resistivity statistics sheet

Item	Electric Resistivity (Ω/m)
Poly-Si	2.52E-4
Poly	0.5E-4
Gate	5.17E-10
SD	2.9E-8
Steel	1.7E-7

2.4 Equivalent electric circuit diagram

ESD process can be abstracted into an equivalent electric circuit diagram (Figure 7), Electrostatic charge is equivalent to a current source. i_s means Electrostatic charge, C_0 means the capacitance formed by EUV tube and SD, r0 means the equivalent resistance of air and capacitance, $\mathcal{R}_{fz}$ means load resistance of conductor connected to SD.

Based on the photoelectric effect and Theory of photon, light intensity formula: $\mathcal{I}=\mathcal{N}\hbar\nu$ [2], $\mathcal{I}$ means light intensity, $\mathcal{N}$ means the photon number, ν means a Planck constant. When EUV illumination is constant, the current excited by the light is constant, and the voltage varies with the load.

2.5 Influencing factors of materials

Based on Ohm's law formula: $\mathcal{U}=i_s \cdot \mathcal{R}_{fz}, = i_s * \rho * \mathcal{L}/S$ [3], larger ρ leads to lager $\mathcal{R}_{fz}$. As a result, the voltage across the conductor is lager. In this formula, $\mathcal{U}$ means the voltage across the conductor, i_s means electrostatic charge, $\mathcal{R}_{fz}$ means load resistance of conductor connected to SD, ρ means the resistivity of the resistance, $\mathcal{L}$ means the length of the resistance, S means the cross-sectional area of the resistance. It can be seen from the chart below (Table 1), the resistivity of Poly-Si is the highest [4],[5]. So, the voltage drop between the Poly-Si terminals is highest. As a result, Poly-Si can be damaged by static electricity very easily (figure 1).

2.6 Influencing factors of areas

According to the antenna effect, the bigger the area of the conductor exposed to the free charge is, the more the charge accumulated is. For SD pattern, the larger the area of the SD pattern is, the more the electrostatic charge is. The SD pattern area on the right side is bigger than the left side (figure 2, where marked green), so the right pattern accumulates more electrical charge, which means i_s is larger. That's why ESD damages only occur on the right side (figure1).

3. Improvement of ESD

With ESD simulation model, we find the key factors which make influence on the electrostatic damage.

Firstly, the density of left and right SD pattern should be kept the same. Secondly, the SD pattern can't be blocky. Thirdly, the light intensity of EUV needs to be reduced in order to reduce the number of excited phonons. Fourthly, the structure of TFT can be optimized to reduce Poly-Si conductivity, in order to mitigate the voltage drop. Fifthly,

optimizing the etching process to reduce free electrostatic charge.

4. Conclusion

The ESD simulation model established in this paper can explain the ESD phenomenon and match the reality very well.With simulation, the quantitative design rules of backplate layout have been formulated. It helps us to save lots of time and cost, which should have been spent on experiment.

5. Acknowledgements

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6. References

[1] David J. Griffiths, Introduction to Electrodynamics, Third Edition [N], World Publishing Corporation, 2006.

[2] Donald A. Neamen, Semiconductor Physics and Devices Basic Principles, Fourth Edition [N], Beijing, Publishing House of Electronics Industry, 2017

[3]Shibai Tong, Chengying Hua, Chaohui Ye, Fundamentals of Analog Electronics,Fifth Edition [N], Beijing, Higher Education Press, 2019

[4] David W. Oxtoby, H. Pat Gillis, Laurie J. Butler, Principles of modern chemistry, Eighth Edition [N], Cengage Learning, 2015

[5] Theodore L. Brown, H. Eugene LeMay, Jr., Bruce E. Bursten, Catherine J. Murphy, Patrick M. Woodward, Matthew W. Stoltzfus, Chemistry: the central Science,13th Edition [N], New York, Pearson Education Inc,2015