Diode-Connected Pixel Circuit with Leakage Current Compensating Mechanism for P-Type LTPS AMOLED Displays

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Keywords: Leakage current, low-frame-rate display, low-temperature polycrystalline silicon thin-film transistor, pixel circuit.

ABSTRACT

This work proposes a pixel circuit with a compensating mechanism of leakage current to mitigate voltage fluctuation at the gate node of the driving TFT. The threshold voltage variation of LTPS TFTs is compensated to generate uniform currents. Therefore, the proposed pixel circuit is suitable for use in low-frame-rate displays.

1 Introduction

Active-matrix organic light-emitting diode (AMOLED) displays are favored by the consumers because of their superior characteristics, such as high contrast ratio, fast response time, thinness, and wide viewing angle [1], [2]. Low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) are widely used to drive OLED devices due to their high driving capability, small layout area, and stable electrical characteristics [3]. Nonetheless, LTPS TFTs suffer from the random distribution of grain boundaries in the channel, causing threshold voltage (V_{TH}) variations [4], [5]. OLED currents generate by the LTPS TFTs-based pixel circuit are non-uniform without any compensating mechanism. Therefore, several pixel circuits have been developed to compensate for the V_{TH} variation and produce uniform driving currents [1], [2], [6], [7]. Goh *et al.* [6] proposed an AMOLED pixel circuit composes of three switching TFTs, one driving TFT, and one capacitor, and compensates for the V_{TH} shift to produce uniform OLED currents. However, the circuit generates current through the OLED device during the pre-charging stage and the data-input stage, causing the flicker phenomenon and decreasing the contrast ratio of the image. The power consumption also increases due to the unexpected current, reducing the use time of the display. To avoid the unexpected current, In *et al.* [8] proposed a simple pixel structure with only two TFTs and one capacitor. The circuit turns ELVSS to high during the reset and programming period to avoid flicker, but the voltage change on the power source lines leads to additional power consumption. Moreover, the data voltage stored in the storage capacitor is continuously coupled by the data line, which will cause the stored data to be distorted and reduce image quality. Power consumption is critical for smartwatch displays since the total power dissipation is higher, and the use time of the smartwatches gets shorter. Therefore, smartwatch displays adopt a low-frame-rate design to reduce the frequency of discharging and charging on the data line by the data source integrated circuit (IC). However, the prolonged emission time will increase the influence of the large leakage currents of the LTPS TFTs on the stored voltage [9]. The amplitude of the driving current is determined by the gate-to-source voltage of the driving TFT, the extended emission time will cause the leakage currents to severely distort the voltage at the gate node of the driving TFT, leading to non-uniform driving currents. Hence, a compensating mechanism for leakage currents of the LTPS TFTs is essential for low-frame-rate displays.

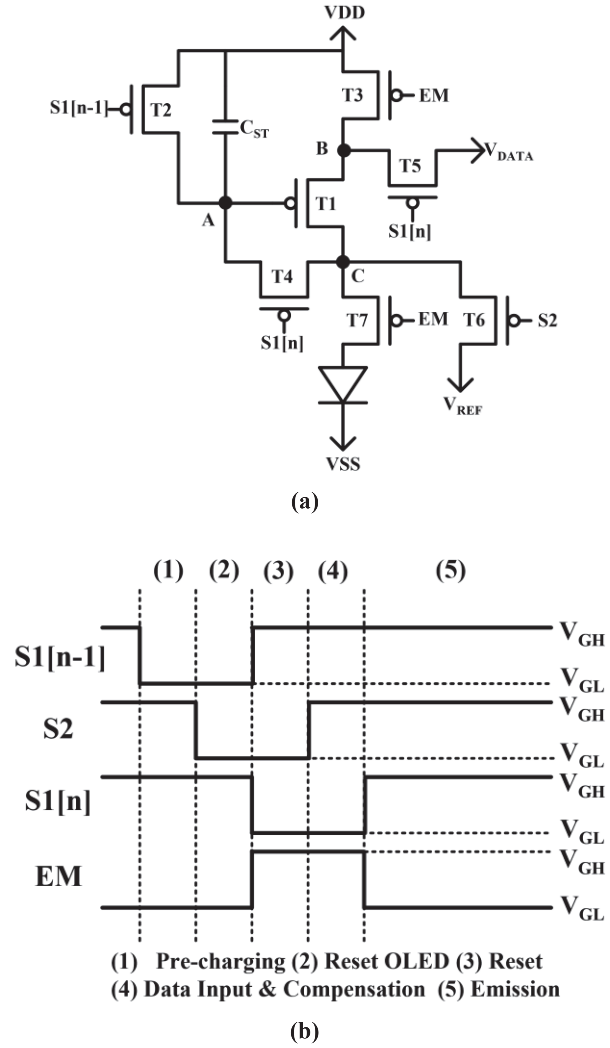

Fig. 1 Proposed pixel circuit. (a) Schematic and (b) timing diagram of control signals.

Table I
PARAMETERS OF PROPOSED PIXEL CIRCUIT

TFT Aspect Ratio and Capacitance			
T1 (μm/μm)	3 / 22	T4 (μm/μm)	3 / (3+3)
T2-3, T5-7 (μm/μm)	3 / 3	C_{ST} (pF)	0.4
Voltages of Signals			
S1, S2 (V)	-4 ~ 5	VDD (V)	3.3
EM (V)	-4 ~ 5	VSS (V)	-3.3
V_{DATA} (V)	2.5 ~ 3.3	V_{REF} (V)	-3.3

This work proposes a pixel circuit based on LTPS TFTs for smartwatch displays with a compensating mechanism of leakage current to alleviate the voltage distortion at the gate node of the driving TFT. The V_{TH} variation of the LTPS TFTs is compensated by the diode-connected structure of the driving TFT. Simulation results indicate that the relative current error rates are all below 4.97% under V_{TH} variations of ±0.5 V, and the maximum voltage variation at the gate node of the driving TFT is 0.065 V. The proposed pixel circuit produces uniform and stable driving currents and thus is suitable for use in low-frame-rate smartwatch displays.

2 Circuit Operation and Driving Scheme

Figs. 1(a) and 1(b) plot the schematic and the timing diagram of the proposed pixel circuit, which contains one driving TFT (T1), six switching TFTs (T2-T7), and one storage capacitor (C_{ST}). Notably, C_{ST} is used to store the data voltage and the sensed V_{TH} for driving TFT. Switching TFTs are controlled by the scan signals S1[n-1], S2, S1[n], and EM. The circuit operation of the proposed pixel circuit and the compensating mechanism of leakage current are divided into two parts, as described in the followings.

2.1 Part A: Operating principles

2.1.1 Pre-charging period

In the first period, S1[n-1] and EM are low to turn on T2 and T3. T2 charges node A to VDD to turn T1 off, ensuring that no current flow through OLED.

2.1.2 Reset OLED period

S2 turns low while S1[n-1] and EM remain low. T6 is turned on and discharges node C to V_{REF}, so the anode of OLED is reset, and OLED is turned off to avoid flicker.

2.1.3 Reset period

During this period, S1[n-1] and EM turn high to turn off T2, T3, and T7. S1[n] and S2 are low to turn on T4, T5, and T6. Nodes A, B, and C are all discharged to V_{REF} to avoid the hysteretic effect on the driving TFT.

2.1.4 Data input & Compensation period

In this period only S1[n] is low, so T4 and T5 are turned on. Therefore, T1 turns into a diode-connected structure and charges node A to V_{DATA}-|V_{TH_T1}| until T1 is cut off, where V_{TH_T1} is the sensed threshold voltage of T1. Notably, the sensed threshold voltage of T1 is stored at C_{ST} for compensation.

2.1.5 Emission period

In the final period, S1[n] turns high to turn T4 and T5 off. EM goes from V_{GH} to V_{GL}, turning T3 and T7 on. T3 charges node B to VDD, and thus T1 is turned on and operated at the

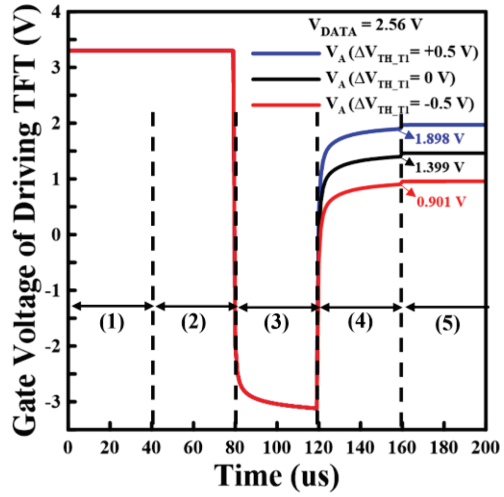

Fig. 2 Transient voltage waveforms of node A with V_{TH_T1} variations of ±0.5 V.

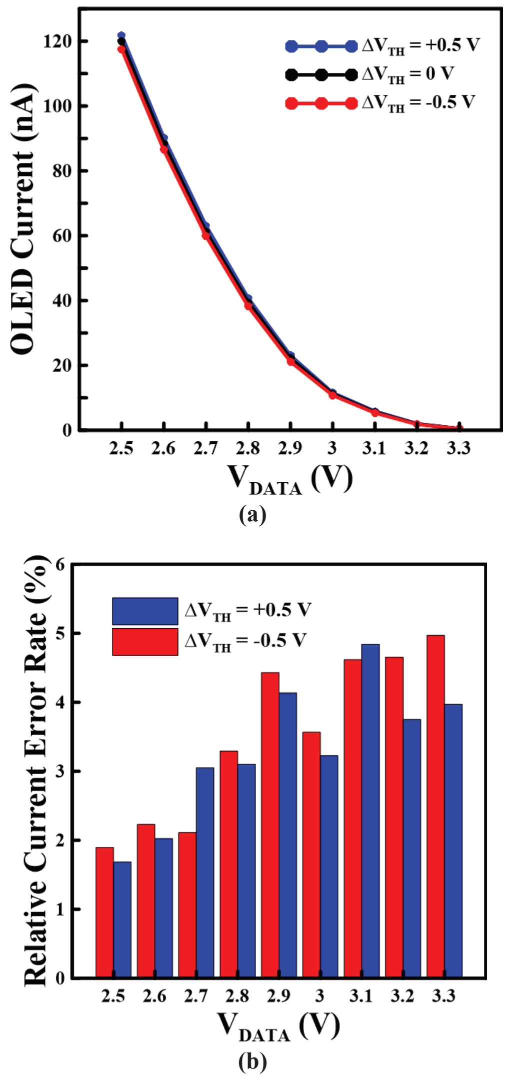

Fig. 3 (a) OLED currents versus data voltage and (b) relative current error rates when ΔV_{TH} are ±0.5 V.

saturation region to generate the driving current. Since the voltage at the gate node of T1 is V_{DATA}-$|V_{TH\_T1}|$ and the voltage at the source node of T1 is VDD. The driving current generated by T1 can be derived as follows:

$$I_{OLED} = \frac{1}{2}k\left(V_{SG\_T1}-|V_{TH\_T1}|\right)^2$$
$$= \frac{1}{2}k\left(V_{DD}-V_{DATA}+|V_{TH\_T1}|-|V_{TH\_T1}|\right)^2$$
$$= \frac{1}{2}k(V_{DD}-V_{DATA})^2 \quad (1)$$

where k is $\mu \cdot C_{OX} \cdot W_{T1}/L_{T1}$ and the I_{OLED} is the OLED current. Eq. (1) is obtained by eliminating V_{TH_T1} from the equation, so the OLED current is independent of the threshold voltage of T1. Therefore, the proposed pixel circuit is immune to the V_{TH} variations of the driving TFT and generates uniform OLED currents.

2.2 Part B: Compensating mechanism of leakage current

After lowering the frame rate to 15 Hz, the emission period is extended to 66.67 ms, and thus leakage current of the LTPS TFTs must be considered. The driving voltage at the gate node of T1, which is stored by C_{ST}, may be severely distorted by the leakage current of T4. Since T1 is operated at the saturation region, node A is discharged by the leakage current of T4, and the OLED current will gradually increase during the prolonged emission period, causing an unstable current. Therefore, T2 is added to compensate for the leakage current. During the emission period, S1[n-1] turns off T2 to provide a compensating leakage current to charge node A. By balancing the discharging leakage current by T2 and the charging leakage current by T4, the distortion at the gate node of the driving TFT can be alleviated. Therefore, the proposed pixel circuit provides uniform and stable driving currents and is suitable for low-frame-rate smartwatch displays.

3 Results and Discussions

To investigate the effectiveness of the proposed pixel circuit the HSPICE simulator with the RPI model (level = 62) is used to simulate the circuit for a 1.41-inch panel with the specifications of resolution of 320×360 and a frame rate of 15 Hz. Table I lists the channel width and length of TFTs, the capacitance of the storage capacitor, the voltage swing of scan signals, the voltage range of V_{DATA}, and the voltage level of the DC sources. Fig. 2 plots the transient waveform of the voltage of node A, which is at the gate node of T1, under V_{TH} variations of ±0.5 V. During the fourth period, node A is charged from V_{REF} to 1.898 V, 1.399 V, and 0.901 V, respectively, so namely the diode-connected structure of T1 senses the V_{TH} variations of +0.499 V and -0.498 V. The proposed circuit successfully detects the V_{TH} variations to generate uniform OLED currents. To show the effectiveness of the V_{TH} compensation, Fig. 3(a) plots the OLED current at each value of V_{DATA} when the V_{TH} of T1 varies by ±0.5 V. The pixel circuit generates uniform OLED current under each gray level after compensating for the V_{TH} variations of T1. Fig. 3(b) shows the relative current error rate of the OLED current when V_{DATA} ranges from 2.5 V to 3.3 V. The maximum current error rate of the proposed circuit under V_{TH} variation of ±0.5 V is 4.96%, proving that the pixel circuit

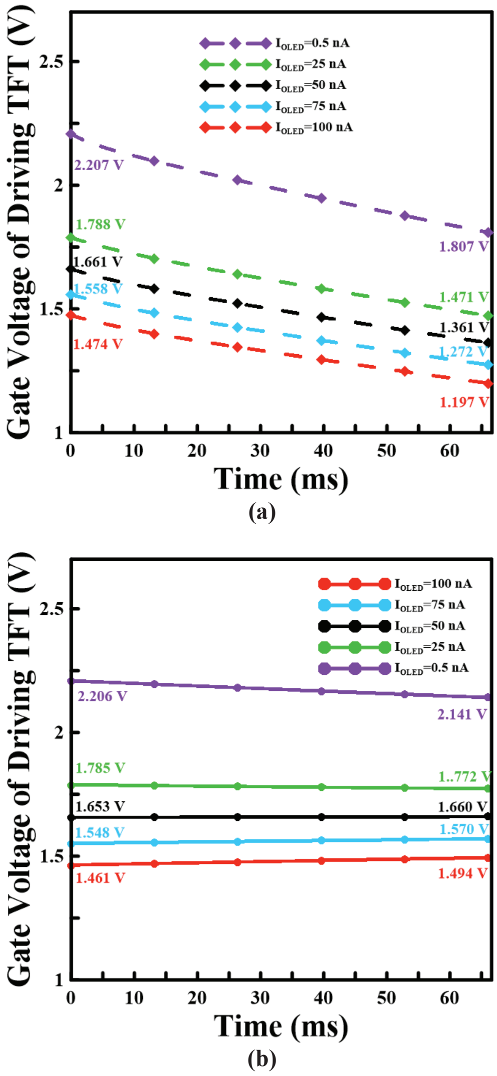

Fig. 4 Variations of voltage at gate node of driving TFT of (a) 4T2C pixel circuit [10] and (b) proposed pixel circuit during emission period.

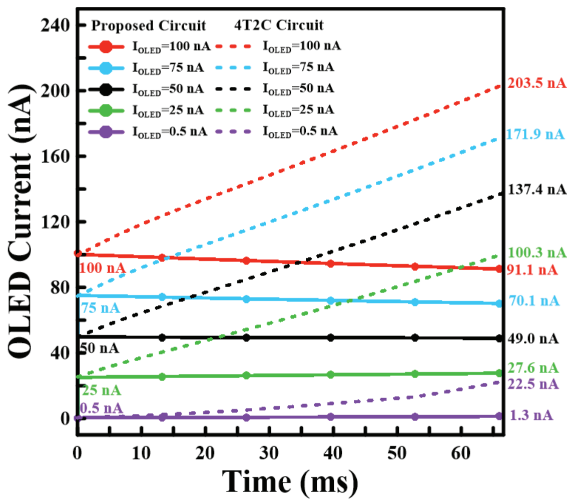

Fig. 5 Comparisons of OLED current variations of proposed circuit and 4T2C pixel circuit [10].

generates uniform current to drive the OLED devices.

To verify the effectiveness of the compensating mechanism of leakage current, the voltage waveform at the gate node of the driving TFT of the proposed pixel circuit is compared with that of the previously developed 4T2C pixel circuit [10]. Figs. 4(a) and 4(b) plot the voltage at the gate node of the 4T2C circuit and the proposed circuit under different initial OLED currents during the emission period. For the 4T2C circuit, without any leakage current compensating mechanism, the voltage gradually drops as the leakage current of the LTPS TFT constantly discharges the gate node, and the maximum voltage variation is 0.4 V. On the contrary, the proposed circuit adopts a compensating mechanism of leakage current. A compensating leakage current balance the discharging leakage current to alleviate the voltage drop at the gate node of the driving TFT and the maximum voltage variation is 0.065 V. Therefore, the voltage variation at the gate node of the driving TFT of the proposed circuit is less than that of the 4T2C circuit under different initial OLED currents, leading to stable OLED currents. Fig. 5 plots the OLED current during the emission period under initial OLED currents of 0.5 nA, 25 nA, 50 nA, 75 nA, and 100 nA of the proposed and 4T2C circuit. Since the 4T2C circuit has no leakage current compensating mechanism, the maximum OLED current variations under different initial OLED currents are 22 nA, 75.3 nA, 87.4 nA, 96.9 nA, and 103.5 nA, respectively. On the contrary, the proposed circuit mitigates the voltage distortion at the gate node of the driving TFT and the maximum OLED current variations are 0.8 nA, 2.6 nA, 1 nA, 4.9 nA, and 8.9 nA. The proposed circuit adopts the compensating mechanism of leakage current and effectively suppresses the OLED current variation, thus significantly improving the image quality.

4 Conclusions

This work presents a pixel circuit with a compensating mechanism for leakage current for low-frame-rate displays. Simulation results show that after compensating for the V_{TH} variation of the driving TFT, the proposed pixel circuit generates uniform OLED currents with current error rates all below 4.97% under V_{TH} variations of ±0.5 V. Furthermore, the voltage distortion at the gate node of the driving TFT caused by the leakage current is alleviated and the maximum voltage variation is 0.065 V, and the OLED current variations of the proposed circuit are greatly decreased compared with that of the previously developed 4T2C circuit. Therefore, the proposed pixel circuit is promising for low-frame-rate displays.

5 Acknowledgement

This work was supported in part by the Advanced Optoelectronic Technology Center, National Cheng Kung University, Tainan, Taiwan, and the Ministry of Science and Technology of Taiwan under Projects of MOST 111-2218-E-006 -011 -MBK, as well as AU Optronics Corporation is appreciated for its technical and funding support.

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