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Therefore, the proposed circuit is appropriate for low-frame-rate AMOLED displays.

2 Circuit Operation and Driving Mechanism

Fig. 1(a) is the proposed AMOLED pixel circuit, and Fig. 1(b) shows the timing diagram of its control signals. This circuit consists of eight TFTs and one capacitor. T4 is the driving TFT, and other TFTs (T1-T3, T5-T8) are the switching TFTs. The circuit operation is divided into the following three stages:

(1) Reset period: SCAN1[n] is low to turn on T1 and T6, and SCAN3[n] is also low to turn on T7. SCAN2[n] and EM[n] are high to turn off T2, T5, and T8. The voltage of nodes A and C are reset to V_{REF} , and node D is charged to V_{DATA} . In the proposed circuit, the current flowing through the OLED is blocked by turning off TFT T8 to suppress flicker phenomenon. Also, T3 is used to achieve leakage compensation, and the gate and source nodes of T3 are connected to V_H to keep T3 turned off at all stages.

(2) Compensation and data input period: SCAN2[n] goes low to turn on T5, and SCAN1[n] remains low to turn on T1 and T6. SCAN3[n] goes high to turn off T7. Hence, T4 becomes diode-connected, and nodes A and C are charged to $V_{DD} - |V_{TH_T4}|$, where V_{TH_T4} is the threshold voltage of T4. Additionally, T1 remains turned on to maintain node D at V_{DATA} , and T8 remains turned off to keep OLED turned off.

(3) Emission period: SCAN1[n] and SCAN2[n] become high to turn off T1, T5, and T6. SCAN3[n] and EM[n] become low to turn on T2, T7, and T8. Node D is charged from V_{DATA} to V_{REF} . Owing to the capacitive coupling effect of C1, the voltage of node A (V_A) is coupled as follows:

$$V_A = V_{DD} - |V_{TH_T4}| + V_{REF} - V_{DATA} \quad (1)$$

where T4 is operated at the saturation region and starts to generate OLED current. Accordingly, the OLED current can be calculated as the following equation:

$$\begin{aligned} I_{OLED} &= \frac{1}{2} k (V_{SG} - |V_{TH_T4}|)^2 \\ &= \frac{1}{2} k [V_{DD} - (V_{DD} - |V_{TH_T4}| + V_{REF} - V_{DATA}) - |V_{TH_T4}|]^2 \\ &= \frac{1}{2} k (V_{DATA} - V_{REF})^2 \end{aligned} \quad (2)$$

where k is $\mu \cdot C_{OX} \cdot W/L$ of T4. As shown in Eq. (2), the V_{TH} of T4 and the power supply voltage, V_{DD} , are eliminated. Therefore, a highly uniform OLED current can be generated by the proposed pixel circuit even if the V_{TH} of TFTs varies or the deviation in V_{DD} occur. Although the OLED current is not affected by the threshold voltage variation and the V_{DD} I-R drop, the large leakage current of LTPS TFTs is still a problem. Due to a low-frame-rate operation applied to the proposed circuit, the emission time is greatly prolonged. The leakage current of the LTPS TFTs will cause the gate voltage of the driving TFT to be distorted at this long emission time, thereby affecting the stability of the OLED current. In order to alleviate the effect of leakage current on the OLED current during the emission time,

Table I
DESIGNED PARAMETERS OF PROPOSED PIXEL CIRCUIT

Parameter	Value	Parameter	Value
(W/L) T1-T3, T5-T8 ($\mu\text{m}/\mu\text{m}$)	3/3	(W/L) T4 ($\mu\text{m}/\mu\text{m}$)	3/22
SCAN1, SCAN2 (V)	-4 - 5	V_{REF} (V)	-1.5
SCAN3, EM (V)	-4 - 5	C1 (pF)	0.4
V_{DD} (V)	3.3	V_{DATA} (V)	-1.53 - -0.81
V_{SS} (V)	-3.3	1 H (μs)	46

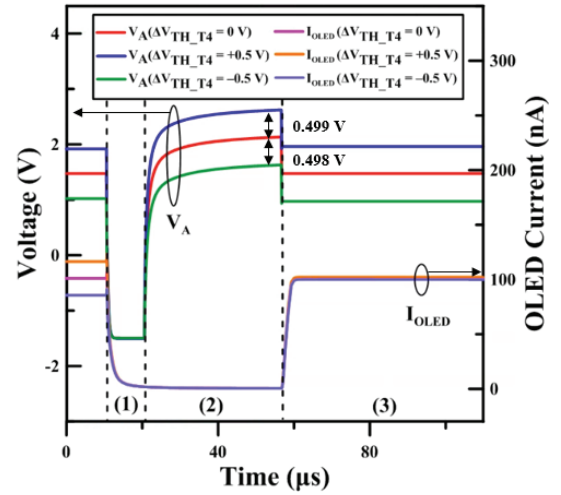
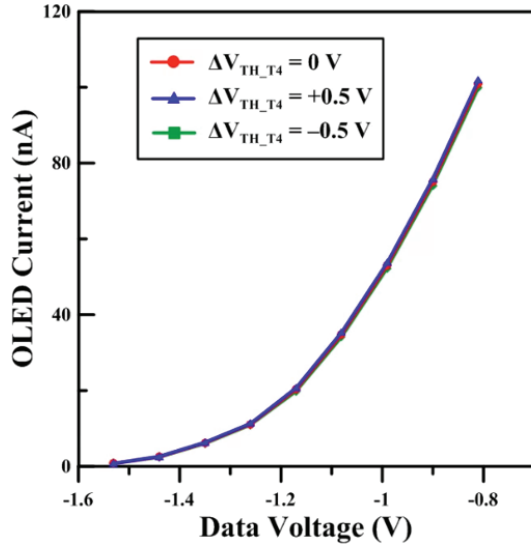


Fig. 2. Transient waveforms of node A and OLED currents as V_{TH} varies by ± 0.5 V.

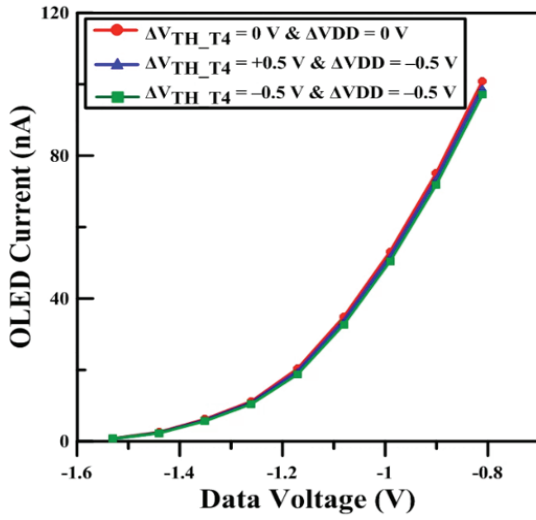
a compensation structure is designed in the proposed circuit. The voltage at node A will be decreased by the leakage path formed by T6 and T7. To compensate for the leakage current, T3 is added to provide the compensating leakage current. Because V_H is higher than V_A , T3 forms a compensation leakage current path. The voltage variation of node A is reduced by balancing leakage currents at node A, enhancing the stability of the OLED current under the emission period. Consequently, the proposed circuit is feasible for low-frame-rate displays.

3 Results and Discussions

To verify the proposed AMOLED pixel circuit for use in a 1.41-inch 320×360 display at the frame rate of 15 Hz, the proposed circuit is simulated by using an HSPICE simulator. Fig. 2 plots the simulated transient waveforms of node A and OLED currents with the V_{TH} variations of driving TFTs are ± 0.5 V. The differences of the voltages at node A at the end of the compensation and data input period are +0.499 V and -0.498 V, which approximates the V_{TH} variation of ± 0.5 V, confirming the compensation capability of the proposed circuit. Fig. 3(a) presents OLED currents versus the data voltages when the V_{TH} variations of the driving TFTs are ± 0.5 V, and



(a)



(b)

Fig. 3. Simulated OLED currents versus data voltages when (a) V_{TH} variations of driving TFTs are ± 0.5 V, and (b) V_{TH} variations of driving TFTs are ± 0.5 V and V_{DD} drops 0.5 V.

Fig. 3(b) shows OLED currents at different data voltages when V_{TH} varies by ± 0.5 V and V_{DD} drops 0.5 V. As shown in Figs. 3(a) and 3(b), neither the V_{TH} variation nor the V_{DD} I-R drop affects the uniformity of the OLED current generated by the pixel circuit. Fig. 4 plots the relative current error rates of the proposed pixel circuit for the TFT V_{TH} variations are ± 0.5 V. The relative current error rates are all below 4.72%, confirming that the proposed circuit can generate high uniformity display images. To verify the feasibility of the leakage current compensation mechanism, the variations in the OLED current of the proposed pixel circuit and the conventional 4T2C pixel circuit under the 66.67 ms emission period are compared in Fig. 5. At low, medium, and high gray levels, the increases of the

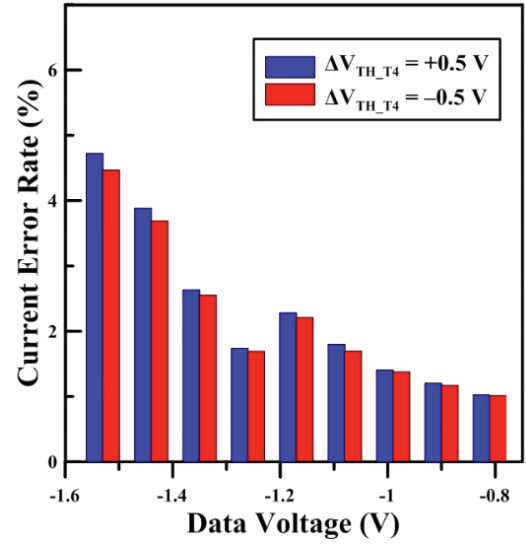


Fig. 4. Relative error rates of OLED currents with V_{TH} variations of ± 0.5 V.

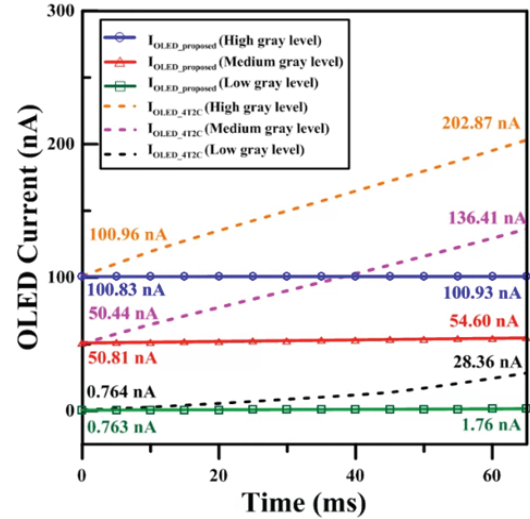


Fig. 5. Variations of OLED currents of proposed pixel circuits and conventional 4T2C pixel circuits during emission time.

OLED currents of the conventional 4T2C circuit are 27.6 nA, 85.97 nA, and 101.91 nA, respectively, under long emission time. In contrast, the OLED current variation of the proposed circuit is only 1 nA, 3.79 nA, and 0.1 nA at low, medium and high gray levels, respectively. The proposed leakage compensation mechanism can successfully compensate for the distortion of the OLED current results from the leakage current. Consequently, the stable images can be obtained in low-frame-rate displays.

4 Conclusions

A new p-type LTPS pixel circuit used in low-frame-rate AMOLED displays is proposed. By using the diode-connected compensation method, the threshold voltage variations and the

V_{DD} I-R drops are successfully compensated. The OLED current distortion caused by the leakage current under the long emission period is alleviated by using the designed compensation mechanism. From the simulation, the relative current error rates of the OLED currents are less than 4.72% with the V_{TH} variations of the driving TFTs are ± 0.5 V. Furthermore, the variations in the OLED current during the emission period were reduced to 1 nA, 3.79 nA, and 0.1 nA at low, medium, and high gray levels, respectively. Consequently, the simulation results verify that the proposed pixel circuit is appropriate for the low-frame-rate AMOLED displays.

Acknowledgments

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References

- [1] H. Y. Lu, T. C. Chang, Y. H. Tai, and P. T. Liu, "A new pixel circuit compensating for brightness variation in large size and high resolution AMOLED displays," *J. Display Technol.*, vol. 3, no. 4, pp. 398–403, (2007).
- [2] C. L. Lin *et al.*, "Compensation Pixel Circuit to Improve Image Quality for Mobile AMOLED Displays," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 2, pp. 489–500, (2019).
- [3] M. Kimura *et al.*, "Low-temperature polysilicon thin-film transistor driving with integrated driver for high-resolution light emitting polymer display," in *IEEE Transactions on Electron Devices*, vol. 46, no. 12, pp. 2282–2288, (1999).
- [4] C. L. Lin, C. C. Hung, P. Y. Kuo, and M. H. Cheng, "New LTPS pixel circuit with AC driving method to reduce OLED degradation for 3D AMOLED displays," *J. Display Technol.*, vol. 8, no. 12, pp. 681–683, (2012).
- [5] C. L. Fan, Y. C. Chen, C. C. Yang, Y. K. Tsai, and B. R. Huang, "Novel LTPS-TFT pixel circuit with OLED luminance compensation for 3D AMOLED displays," *J. Display Technol.*, vol. 12, no. 5, pp. 425–428, (2016).
- [6] R. Dawson, Z. Shen, D.A. Furst, S. Connor, J. Hsu, M.G. Kane, R.G. Stewart, A. Ipri, C. N. King, P. J. Green, R. T. Flegal, S. Pearson, W. A. Tang, S. Van Slyke, F. Chen, J. Shi, M. H. Lu, and J. C. Sturm, "The impact of the transient response of organic light emitting diodes on the design of active matrix OLED displays," *IEDM Tech. Dig.*, pp. 875–878, (1998).
- [7] W. J. Wu, L. Zhou, R. H. Yao, and J. B. Peng, "A new voltage programmed pixel circuit for enhancing the uniformity of AMOLED displays," in *IEEE Electron Device Letters*, vol. 32, no. 7, pp. 931–933, (2011).
- [8] N. H. Keum, K. Oh, S. K. Hong, and O. K. Kwon, "A pixel structure using block emission driving method for high image quality in active organic light-emitting diode displays," *J. Display Technol.*, vol. 12, no. 11, pp. 1250–1256, (2016).
- [9] C. L. Lin *et al.*, "Leakage-Prevention Mechanism to Maintain Driving Capability of Compensation Pixel Circuit for Low Frame Rate AMOLED Displays," in *IEEE Transactions on Electron Devices*, vol. 68, no. 5, pp. 2313–2319, (2021).
- [10] C. L. Lin, J. H. Chang, P. C. Lai, L. W. Shih, S. C. Chen, M. H. Cheng, "Pixel circuit with leakage prevention scheme for low-frame-rate AMOLED displays," in *IEEE Journal of the Electron Devices Society*, vol. 8, pp. 235–240, (2020).
- [11] J. H. Park, K. H. Seok, H. Y. Kim, H. J. Chae, S. K. Lee and S. K. Joo, "A Novel Design of Quasi-Lightly Doped Drain Poly-Si Thin-Film Transistors for Suppression of Kink and Gate-Induced Drain Leakage Current," in *IEEE Electron Device Letters*, vol. 36, no. 4, pp. 351–353, April (2015).
- [12] C. S. Lin, Y. C. Chen, T. C. Chang, S. C. Chen, F. Y. Jian, H. W. Li, T. C. Chen, C. F. Weng, J. Lu, and W. C. Hsu, "Anomalous capacitance induced by GIDL in p-channel LTPS TFTs," in *IEEE Electron Device Letters*, vol. 30, no. 11, pp. 1179–1181, (2009).