Pixel Circuit with Series-Connected Leakage Current Prevention Structure for AMOLED Displays

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ABSTRACT

An AMOLED pixel circuit used for low frame rate application is proposed in this article. The relative error is suppressed within 3.08% under threshold voltage variation of driving TFT. The variation of driving current decreases to 8.16 nA when emission time is prolonged to 66.67 ms.

1. Introduction

In recent years, active-matrix organic light-emitting diode (AMOLED) display is the mainstream technology, owing to the great contrast ratios, wide viewing angles, high brightness, and flexibility [1]-[3]. Low-temperature poly-crystalline silicon thin-film transistors (LTPS TFT) with superior driving capability as are commonly used as the backplane of AMOLED displays to generate the driving current. However, the non-uniform electrical characteristics of LTPS TFTs are a critical issue for image quality [4] – [6]. A few previous pixel circuits are presented and focused on the compensation structure for threshold voltage (V_{TH}) variations of LTPS TFTs. Lin *et al.* gave an AMOLED pixel circuit that used the overlapping signals to prolong the compensation time [7]. The variations of V_{TH} are sensed successfully during the enough compensation time in this circuits. Nevertheless, the intrinsic parasitic resistance of power lines causes the voltage drops in VDD lines (VDD I-R Drops), bringing the fluctuation of the driving current [8], [9]. Additionally , as the AMOLED display applications are expanded to smartwatches and wearable displays, the frame rate are decreased to reduce the charging frequency of driver integrated circuit (IC), lowering the power consumption to increase the usage time [10] – [11]. Thus, the stored driving voltage may be distorted severely by the leakage current of switching TFTs due to the extended emission time. The conventional pixel circuit demonstrated by Dawson *et al.* used the diode-connected structure to eliminate the influence of V_{TH} variations [12]. However. when the emission time is increased, the driving voltage of the TFT leaks from the gate node to the cathode of OLED through the switching TFT which is employed to compensate, resulting in the nonuniformity of luminance.

This work proposed an AMOLED pixel circuit that consists of ten TFTs and two capacitors (10T2C). To solve the problems of V_{TH} variations and VDD I-R drops, the diode-connected structure is adopted. Moreover, the leakage of driving voltage can be compensated by the leakage prevention circuit. Simulation results based on the 1.41-inch and 15 Hz frame rate AMOLED display are given in the following sections, and the comparison between the conventional circuit (4T2C) and the proposed circuit within the 66.67 ms emission time is also revealed to verify the reliability of this work.

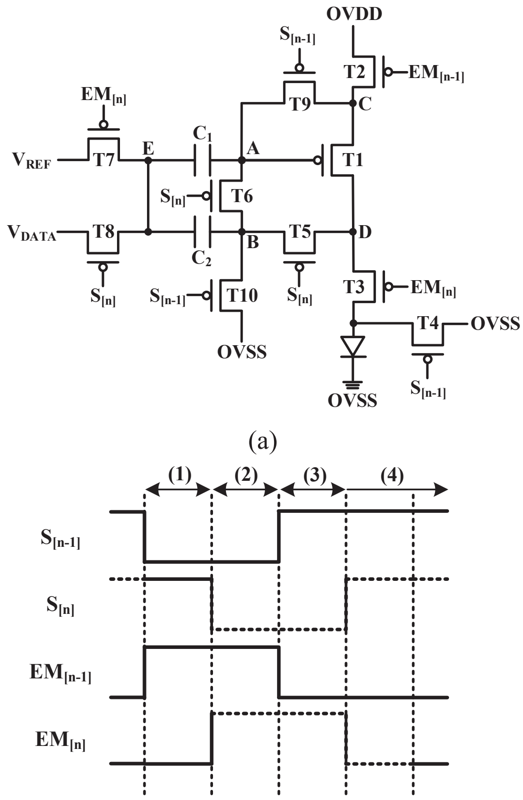


Fig. 1. (a) The structure and (b) the timing diagram of the AMOLED pixel circuit in this article.

Table I

PARAMETERS OF PROPOSED CIRCUIT AND THE CIRCUIT [12]

Proposed Circuit			
VDD (V)	3.3	$(W/L)_{TOLED}$ (μm)	3/22
VSS (V)	-3.3	$(W/L)_{T1}$ (μm)	3/22
V_{REF} (V)	1.2	$(W/L)_{T2\sim T10}$(μm)	3/3
V_{DATA} (V)	1.15~1.88	C_1/C_2(pF)	0.3/0.1
SCAN (V)	-4~5	C_{OLED} (pF)	0.2
Compared circuit □			
VDD (V)	3.3	$(W/L)_{TOLED}$ (μm)	3/22
VSS (V)	-3.3	$(W/L)_{Tdri}$ (μm)	3/22
V_{DATA} (V)	1.95~3.42	$(W/L)_{Tsw}$(μm)	3/3
SCAN (V)	-4~5	C_{OLED} (pF)	0.2
C_{total} (pF)	0.4		

2. Proposed Circuit and Operation

Figs. 1(a) and (b) show the AMOLED pixel circuit and corresponding timing diagram. T1 is the driving TFT to generate the driving current, and the driving voltage is stored at C1. The operations of the proposed circuit are divided into reset OLED period, data input period, compensation period, and emission period. The detailed descriptions are expressed as follows.

2.1 Reset OLED period

$S_{[n-1]}$, and $EM_{[n]}$ are at a low-level voltage (V_{GL}), and thus T3, T4, T7, T9, and T10 are turned on. The voltages of node B (V_B) and node E (V_E) are equal to OVSS and V_{REF}, respectively. The anode of OLED is reset to OVSS to prevent the flicker phenomenon.

2.2 Data input period

$S_{[n]}$ goes to V_{GL} to turn on T5, T6, and T8. $EM_{[n]}$ is turned to a high-level voltage (V_{GH}), so T3 and T7 are at off-state. The nodes A, B, and D are set at OVSS. Meanwhile, the data voltage (V_{DATA}) whose magnitude determines the grayscale is applied to node E. Notably, the OLED is still turned off to avoid additional power consumption.

2.3 Compensation period

As $EM_{[n-1]}$ is changed from V_{GH} to V_{GL}, T2 is turned on. Therefore, through the diode-connected structure of T1, node A is charged to OVDD-$|V_{TH\_T1}|$ until T1 is turned off. V_E keeps at the same V_{DATA} value as the data input period to hold the charges stored in the capacitors. The voltage crosses C_1 can be described as the following equation:

$$V_{C1} = OVDD - |V_{TH\_T1}| - V_{DATA} \tag{1}$$

The $|V_{TH\_T1}|$ and the VDD I-R drop are both sensed in C_1 to compensate for the variations that would affect the driving current (I_{OLED}).

2.4 Emission period

$EM_{[n-1]}$ and $EM_{[n]}$ are both at V_{GL} to turn on T2, T3, and T7. V_{REF} is delivered to node E, and thus while node A is floating, the voltage of node A (V_A) is coupled to V_{REF}-V_{DATA}+OVDD-$|V_{TH\_T1}|$ by the charge conservation of C_1. T1 is consequently turned on, and the driving current shown below flows through the OLED.

$$\begin{aligned} I_{OLED} &= \frac{1}{2}k(V_{SG1} - V_{TH\_T1})^2 \\ &= \frac{1}{2}k\left(OVDD - (V_{REF} - V_{DATA} + OVDD - |V_{TH\_T1}|) - |V_{TH\_T1}|\right)^2 \\ &= \frac{1}{2}k(V_{DATA} - V_{REF})^2 \end{aligned} \tag{2}$$

k is the $\mu \cdot C_{ox} \cdot W/L$ of T1. In the Eq. (2), the driving current is modulated by the V_{DATA} and V_{REF} only, ensuring the influences of V_{TH} and VDD I-R drop are compensated. When the emission time is prolonged in the smart-watch applications, V_A may decrease gradually due to the leakage current of the switching TFTs (T5, T6 and T10) from V_A to OVSS, causing the fluctuation of OLED current. Hence, the proposed circuit utilizes a compensation structure of T9 which provides the compensating leakage current that flows from OVDD to V_A to suppress the variation of V_A. Meanwhile, C_2 is used to slow down the speed of leakage current to achieve the balance of the compensating leakage current and leakage current.

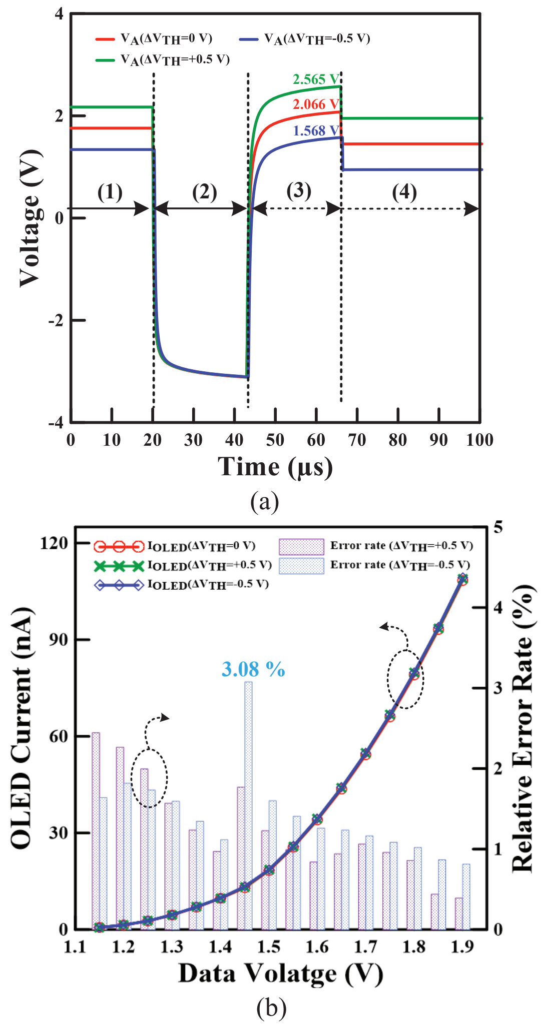
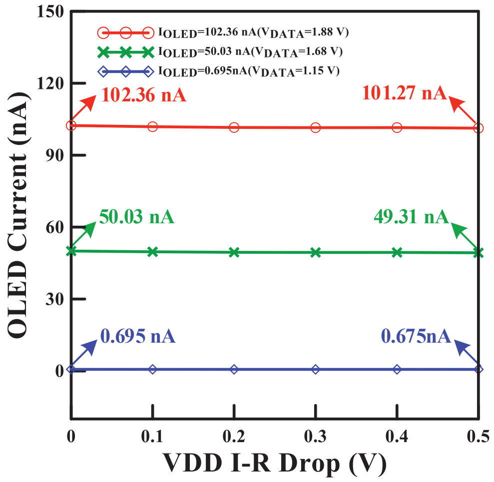


Fig. 2. (a) Transient waveforms of V_A, and (b) I_{OLED} and relative error rate versus data voltages when V_{TH} varied ±0.5 V.

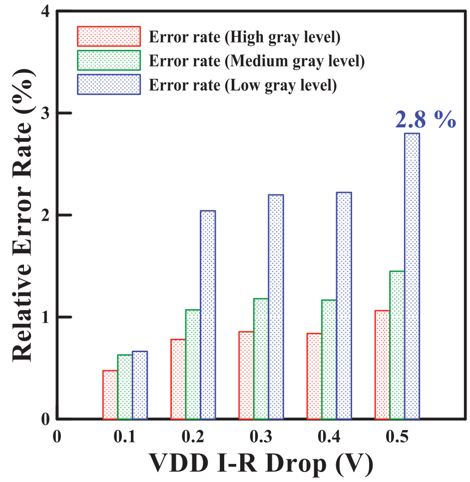
The proposed AMOLED pixel circuit eliminates the effects of V_{TH} variation and VDD I-R drops, improving the uniformity of the driving current. To stabilize the driving current during extended emission time, the compensation structure with leakage current prevention is adopted, increasing the feasibility for use in smart watch displays.

3. Simulation Results and Discussions

The electrical characteristics measurements of LTPS TFTs are provided by the collaborative company, and those are equivalent to the fitted model that used the Rensselaer Polytechnic Institute poly-silicon TFT model (Level 62) in HSPICE simulator. Based on a 1.41-inch AMOLED smartwatch display with a frame rate of 15 Hz and resolution of 320 × 360, the simulation parameters are designed as shown in Table I, including

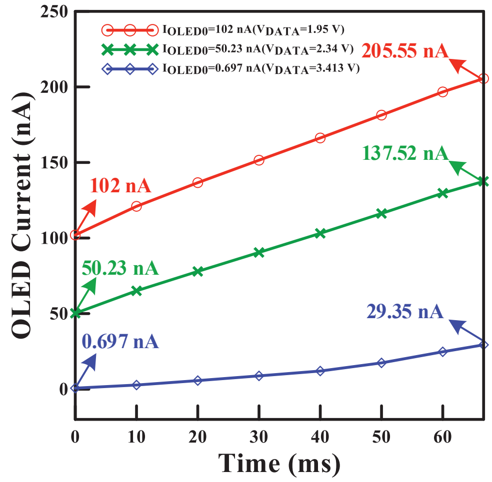


(a)

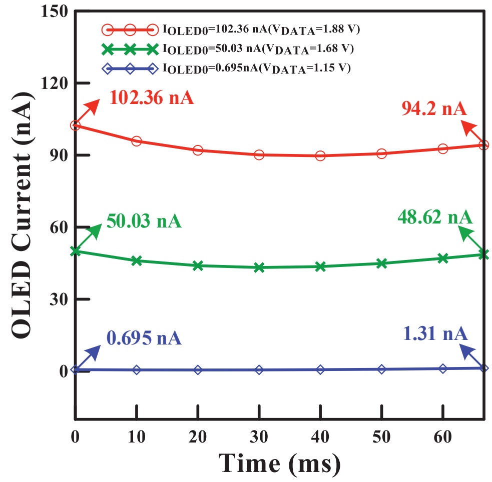


(b)

Fig. 3. (a) IOLED and (b) the relative error rate as VDD I-R drop is from 0 V to 0.5 V.



(a)



(b)

Fig. 4. (a) IOLED of 4T2C and (b) IOLED of 10T2C within emission time of 66.67 ms.

the aspect ratio of TFTs, capacitance of capacitors, and swings of control signals. To emulate the electrical characteristics of OLED, a driving TFT with a diode-connected structure (T_{OLED}) is in parallel with a capacitor (C_{OLED}). Fig. 2(a) plots the transient waveform of node A during each period. When the V_{TH}s of T1 are varied by $\pm$0.5 V, the variations of node A are 0.499 V and -0.498 V at the end of the compensation period which are almost equal to the V_{TH} variations. These results proved the V_{TH} variations of T1 can be sensed successfully and stored at the C_1. Fig. 2(b) gives the driving currents and the relative error rates versus different data voltages. The driving currents in V_{TH} variations of $\pm$0.5 V still remain highly uniform, and the corresponding relative error rates are defined shown as below:

$$Error\ rate = \frac{|I_{OLED\_WO} - I_{OLED\_W}|}{I_{OLED\_WO}} \times 100\% \qquad (3)$$

I_{OLED_wo} represents the driving current without any variations, and I_{OLED_w} is the driving current with variations such as V_{TH} variations or VDD I-R drops. The maximum relative error rate is 3.08 % at V_{DATA} of 1.45 V when V_{TH} of T1 is varied by -0.5 V, verifying the driving current of the proposed circuit is immune to the effects of V_{TH} variations. Moreover, Fig. 3(a) illustrates the variations of I_{OLED} as the VDD drops by 0.5 V. I_{OLED}s only decreased by 1.09 nA, 0.72 nA, and 0.02 nA, respectively, in high, medium, and low gray levels. According to the Eq. (3), the relative error rates can be evaluated as Fig. 3(b). In spite of the VDD I-R drop of 0.5 V, the relative error rates are below 2.8 % in every grayscale. The compensation performance of the proposed circuit is validated, improving the uniformity of the driving current. As the emission time is extended to 66.67 ms in this work, the variation of driving current would be discussed. The conventional 4T2C pixel circuit without leakage prevention structure is a compared target with the proposed circuit. To ensure a fair comparison, the parameters in both circuits are set identically, listed in Table I. Fig. 4(a) and (b) are the driving currents of the 4T2C circuit and the proposed circuit within an emission time of 66.67 ms, and the initial values of the driving current (I_{OLED0}) are similar for reasonable analysis. Without the leakage compensation structure, the I_{OLED}s of the 4T2C circuit are changed severely, and the maximum variation of I_{OLED}s reaches 103.55 nA at the high gray level that causes non-uniform luminance of images. Conversely, as shown in Fig. 4(b), I_{OLED}s of proposed circuit at high, medium, and low gray levels are varied by 8.16 nA, 1.41 nA, and 0.615 nA, greatly improving the fluctuations of I_{OLED}s than the 4T2C circuit. The proposed circuit eliminates the variation of V_{TH} and VDD I-R drops and also maintains the driving current during the prolonged emission time by the leakage-prevention structure.

4. Conclusions

This work presented an AMOLED pixel circuit that is applicable to the smartwatch display with a low frame rate. The driving current is independent of V_{TH} variation and voltage drops of power line to increase the uniformity of images. The simulations show the relative error rates under the V_{TH} variation and VDD I-R drops are less than 3.08% and 2.8 %, respectively. Through the leakage-prevention structure of this work, the maximum variation of driving current is suppressed within 8.16 nA during the emission time of 66.67 ms. Hence, the proposed AMOLED pixel circuit improves the image quality for use in smartwatch applications, enhancing the added value of AMOLED displays.

Acknowledgments

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