Controlling impedance matching in RF reflectometry measurement of quantum dot via FPGA

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Silicon quantum dots (QDs) are a promising candidate for quantum computation thanks to its long coherence time [1] and compatibility with CMOS technology [2,3]. RF reflectometry is used to read out the quantum state in the QDs to obtain a high bandwidth in the measurement. Devices with a global top gate provide significant advantages such as inducing carriers at smaller threshold voltage. However, a relatively large gate area can cause a remarkable change in resistance and the capacitance, disturbing impedance matching in RF reflectometry measurement. To overcome this problem, we connect a single voltage-tunable capacitor (varactor) to our device and the matching network in parallel and dynamically control impedance matching via FPGA to have good impedance matching as shown in Fig. 1.

In our setup, we mainly focus on the change of the capacitance of the device which emerges when the top gate voltage (V_{tg}) is swept. First, we measure V_{tg} and then use an approximate function to tune the varactor voltage accordingly to have good impedance matching during the measurement (Fig.2). We confirmed good impedance matching on this setup.

In addition, since the operation of FPGA at cryogenic temperature has been confirmed [4], in the future FPGA can be located at the same temperature with quantum dot to reduce the heat of cables connected to FPGA.

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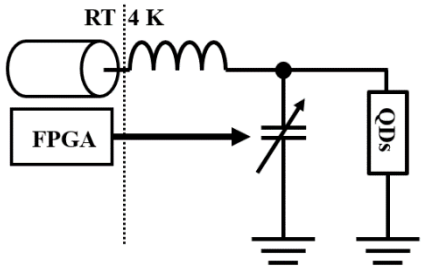

Fig. 1 A schematic of impedance control circuit

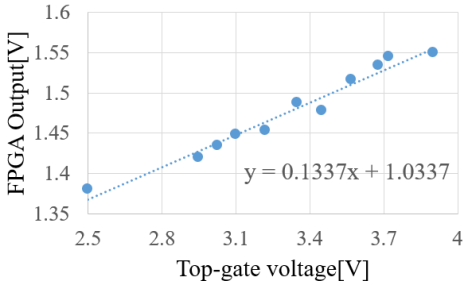

Fig. 2 Output voltage vs Top gate voltage