

## Local thickness tuning (or adjustment) of SOI layer by $\mu$ -transfer printing

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Within the last decade, silicon photonics has been established as a leading position among various photonics integration platforms. Compared with existing heterogeneously integrated approaches such as wafer and chip bonding),  $\mu$ -transfer -printing technology has highly gained interest due to its parallel transfer of multiple devices [1]. This technique utilizes the viscoelastic properties of elastomeric materials, polydimethylsiloxane (PMDS), to pick up the device individually or massively from the substrate and then print on a silicon photonics wafer with high alignment accuracy. In this work, we propose an approach to construct an efficiently coupling scheme by transferring an adiabatic silicon taper onto another silicon waveguide which allows us to control the thickness of any SOI platforms.

To obtain an efficient coupling scheme, the effective refractive index of silicon waveguide should be gradually larger than III-V waveguide. Therefore, a thicker silicon waveguide (500 nm) provides tight mode confinement and efficient mode filed transfer [2]. Figure 1 shows the schematic diagram of the proposed taper design. An additional silicon layer (Layer-2) is transferred onto the original SOI platform (Layer-1) to locally increase the thickness before integrating the III-V devices. To reduce the mode mismatch between the III-V membrane and silicon waveguides, adiabatic tapers are installed to obtain the smooth mode transfer. In this way, we can suppress the coupling loss below -0.5 dB at a taper tip width of 200 nm, while less than -1.0 dB was the upper limit with a standard 220 nm SOI platform. The misalignment tolerance along the Y-direction is about 0.2  $\mu\text{m}$  with a 1 dB decrease in transmittance, as shown in Figure 2.

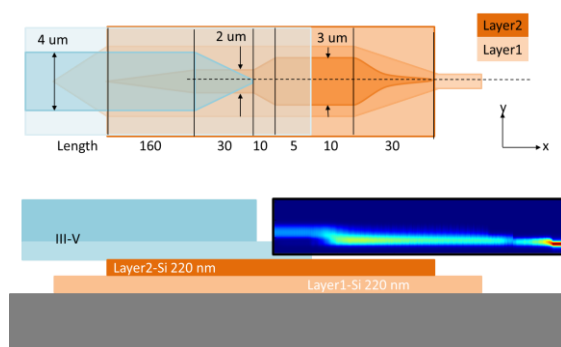


Figure. 1 The schematic diagram of dual silicon layer converter and cross-sectional mode evolution.

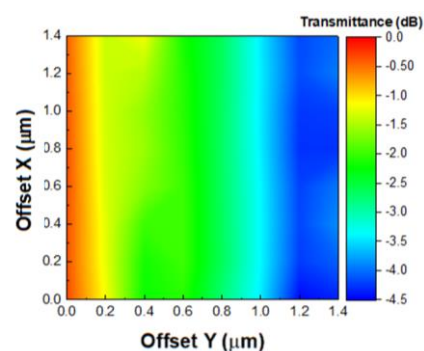


Figure. 2 The transmittance of misalignment between III-V and silicon layer

### Reference

1. R. Kou, et. al., Opt. Express **28**, 19772-19782 (2020).
2. T. Ferrotti, et. al., IEEE Photonics Technology Letters, **28**, 1944-1947(2016).