Realization and Characterization of Vertical Ge n^+/p Structure Towards Nanowire Transistor Applications

NIMS - MANA[1], Univ. of Tsukuba - Applied Physics[2]
°Rahmat Hadi SAPUTRO[1,2], Ryo MATSUMURA[1], Naoki FUKATA[1,2]
E-mail: s1920355@s.tsukuba.ac.jp

Introduction

The excellent transport properties of Ge make it a prime candidate for next-generation CMOS-compatible electronic devices. A crucial problem in making n-MOSFET is the difficulties to form high quality n^+ Ge for the source/drain [1-2]. In this research, we are focusing on the study of vertically structured Ge n^+/p junction fabricated by MBE. Realization of vertical Ge p-n junction is promising for the development of nanowire transistor. Here, the effect of junction scaling to the performance of n^+/p diodes are investigated by a conventional current-voltage measurement.

Experimental Section

An epitaxial Ge layer (100 nm) with high Sb doping ([Sb]: 2×10^{20} and 7×10^{20}cm^{-3}, measured by SIMS) was deposited on p-Ge (100) substrate using an optimized MBE condition. Then, the samples are patterned using photolithography, followed by dry etching in CF4 plasma to form vertical n^+/p junction structure shown in Fig.1(a). Sizes and shapes of the fabricated diodes are shown in Fig.1(b).

Results and Discussion

Well-behaved Ge p-n diodes were confirmed by the I-V curve measurements ($I_{ON}>I_{OFF}$). In Fig.2, the increase of diode performance (I_{ON}/I_{OFF} ratio) by nearly 2-orders of magnitude was obtained by reducing the junction area by 0.01 times. This improvement is the result of significant I_{OFF} reduction as shown in the inset of Fig.2. The high I_{OFF} in larger samples indicates the high current leakages, which remarkably suppressed in smaller samples. Top performance of $I_{ON}/I_{OFF} = 2.6\times10^2$ was obtained on samples with higher Sb concentration ([Sb]: 7×10^{20}cm^{-3}) and might possibly increases by further scaling down of junction area.

[1] W. Kim et al. *IEEE Trans. Elec. Dev.* ***61***, (2014). [2] D.V. Yurasov et al. *J. Cryst. Growth* ***491***, (2018).

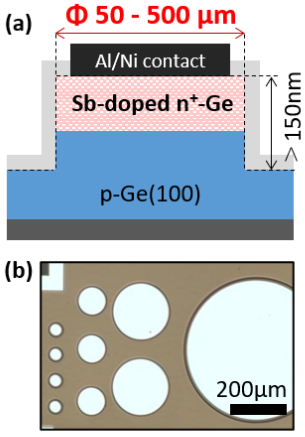

Fig 1. (a) Schematic diagram of the sample. (b) Top-view of the Nomarski microscopic image.

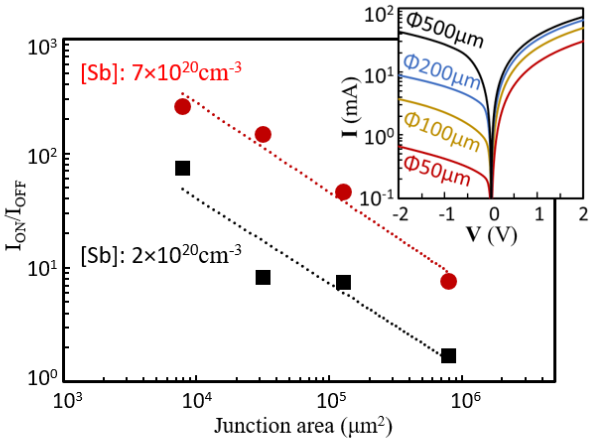

Fig 2. Diode performance (I_{ON}/I_{OFF} at ±2V) as a function of junction area. (Inset shows I-V curves of diode with [Sb]: 2×10^{20} cm^{-3})