

界面ディラック電子に起因した磁気異方性に基づく電圧制御磁化反転

Voltage-control of magnetization reversal based on magnetic anisotropy originating from interfacial Dirac electrons

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Electrical control of magnetization is essential for the next-generation spintronic technologies such as nonvolatile magnetic memory. In particular, the voltage-control of the magnetic anisotropy (VCMA) in ferromagnets promises an energy-efficient reversal of magnetization based on the clocking scheme, which earlier has been demonstrated by using a pulsed voltage in magnetic tunnel junction (MTJ). However, the VCMA method in MTJ still requires a high gate voltage and a constant-bias magnetic field, which is a disadvantage for practical applications. In contrast, as another important method for magnetization reversal, current-induced spin-orbit torque (SOT) in topological insulator (TI) based magnetic heterostructures has been studied in recent experiments [1], which succeeded in reducing the switching power consumption by current pulse injected parallel to a bias magnetic field [2].

In this research, inspired by the VCMA and SOT approaches for magnetization control, we combine them and present two distinct clocking methods for the magnetization switching in TI based magnetic heterostructures [3]. First, we analytically formulate the uniaxial magnetic anisotropy in magnetic TIs as a function of the Fermi energy. Next, as shown in Fig. 1, we propose a transistor-like device with the functionality of a nonvolatile magnetic memory adopting the VCMA writhing method that require no external magnetic fields and the anomalous-Hall-effect based readout scheme. For the magnetization reversal, the estimated source-drain current density and gate voltage are the orders of 10^4 - 10^5 A/cm² and 0.1V, respectively, which are much smaller than those of traditional heavy-metal/ferromagnet heterostructures as well as the MTJs. We also discuss the possibility of using the proposed method for magnetization reversal in TI/ferromagnetic-insulator bilayers with magnetic proximity at the interface.

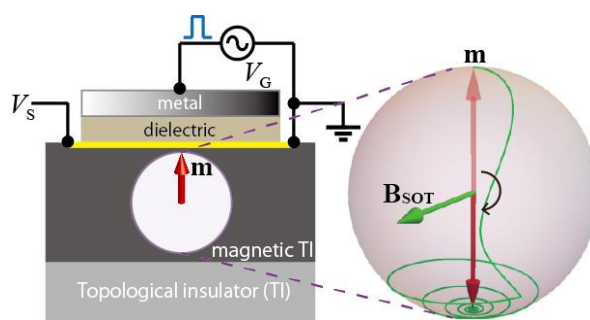


FIG. 1. Schematic geometry (side view) of field-effect transistor (FET)-like device. **m** denotes magnetization vector.

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- [2] K. Yasuda *et al.*, Phys. Rev. Lett. **119**, 137204 (2017).
- [3] T. Chiba and T. Komine, Phys. Rev. Appl. **14**, 034031 (2020).