Al_2O_3/SiO_2 界面ダイポール層形成による 4H-SiC MOS キャパシタの正方向 V_{FB} シフト
Positive V_{FB} shift of 4H-SiC MOS capacitors induced by Al_2O_3/SiO_2 interface dipole layer formation

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[Introduction] Generally, threshold voltage (V_{th}) of SiC-MOSFET is tuned by the channel doping concentration, however, an intentional increase in the doping concentration to achieve a sufficiently large V_{th} can cause a significant deterioration of channel conductance [1]. Introduction of negative fixed charges at SiO_2/4H–SiC interface may also contribute to the positive shift of V_{th}, but this might have some influence on its reliability. Therefore, additional novel processes are demanded for the increase of V_{th} while maintaining the oxide-semiconductor interface quality or channel mobility of MOSFETs. In this work, we demonstrated the formation of an additional dipole layer on top of SiO_2 for the control of flat-band voltage (V_{FB}) of SiO_2/4H-SiC MOS capacitors. We have already clarified the dipole layer formation at SiO_2/SiC interface by interface nitridation [2], but in this work we are going to manipulate the dipoles formed in the gate dielectric layer by using Al_2O_3/SiO_2 interface [3].

[Experiments] N-type 4H-SiC 4°-off (0001) Si-face wafers with epitaxial layers (N_D ~ 1.0×10^{16} cm^{-3}) were used as the substrates. After cleaning and HF etching, samples were thermally oxidized at 1300°C to grow SiO_2 layers in oxygen ambient. After oxidation, NO-POA processes at 1150°C in the ambient of NO:N_2=1:2 were performed. After a slight sacrificial etching of the surface of SiO_2 with 0.1% HF (<1 nm), Al_2O_3 thin film was sputtered on top of SiO_2 using Al_2O_3 ceramic target. After Al_2O_3 deposition, post-deposition annealing (PDA) was conducted at 800°C in 0.1% O_2 + N_2 ambient. Au and Al were used as top and bottom electrodes, respectively. From C-V measurements, the V_{FB} of each MOS capacitor was estimated. After C-V measurements, D_{it} was estimated by using the conductance method. Al_2O_3 thickness was determined by X-ray reflectivity.

[Results & Discussions] **Figure 1** shows the bidirectional C-V curves measured at 1 MHz before and after ~3.3 nm-thick Al_2O_3 sputtering. V_{FB} for all the samples were reasonably extracted since they show nearly ideal curves with small frequency dispersions. **Figure 2** shows the comparison of the V_{FB} as a function of capacitance equivalent thickness (CET) between SiO_2/SiC (black) and Al_2O_3(~3.3 or ~6.6 nm)/SiO_2/SiC (colored) systems. The thickness of SiO_2 was around ~17 or ~32, or ~40 nm, respectively. Due to the small variation of SiO_2 thickness after thermal oxidation even though the samples oxidized at the same condition, there was some total thickness variation. First, for SiO_2/SiC (black points and line), the line was almost flat, which indicates low fixed charges at the SiO_2/SiC interface after nitridation. Next, for Al_2O_3/SiO_2/SiC (colored) samples, we can observe the increased V_{FB} (0.6~0.8 V), induced by the dipole layer at the Al_2O_3/SiO_2 interface [3]. With the increase of Al_2O_3 thickness, clearly there was almost no change of V_{FB}, which can be strong evidence of the non-significant fixed charge formation at Al_2O_3/SiO_2 interfaces. Therefore, the origin of positive V_{FB} shift would be the dipole layer at the Al_2O_3/SiO_2 interface. In order to clarify that Al_2O_3 fabrication processes had no impact on the SiO_2/4H-SiC interface, we estimated the interface state density (D_{it}) before and after Al_2O_3 deposition. **Figure 3** shows the D_{it} for the MOS capacitors with and without the Al_2O_3 layer on top, followed by PDA. We could observe that there was almost no change of D_{it} after the Al_2O_3 fabrication process. From these results, positive V_{FB} shift can be achieved only by the introduction of a few nanometer Al_2O_3 on top, while maintaining the MOS interface quality.

[Conclusions] To achieve higher V_{FB}, we deposited very thin Al_2O_3 layers on top of thermally oxidized SiO_2. Thanks to the interface dipole layer effects at $Al2O_3/SiO_2$, we successfully fabricated Al_2O_3/SiO_2/4H-SiC MOS capacitors with higher V_{FB} than SiO_2/4H-SiC MOS capacitors (~0.8 V), while maintaining the SiO_2/SiC interface quality. Considering that multilayer stack ($Al_2O_3/SiO_2/Al_2O_3$…) is expected to increase V_{FB} further, which has been already demonstrated on Si MOS capacitor [3], this technique can be a great option for the nitrided SiC devices against the unwanted negative shift of V_{FB} which is often introduced by typical nitridation processes [4].

References [1] M. Noguchi et al., IEDM Tech. Digest p.185 (2018). [2] T. H. Kil and K. Kita, Appl. Phys. Lett. 116, 122103 (2020). [3] H. Kamata and K. Kita, Appl. Phys. Lett. 110, 102106 (2017). [4] G. Chung et al., Appl. Surf. Sci. 184, 399 (2001).

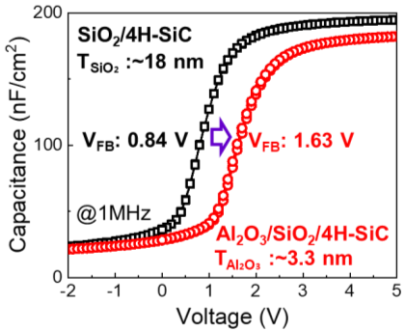

Fig.1 1MHz Bidirectional C-V curves of SiO_2/SiC MOS capacitors with and without Al_2O_3 thin film.

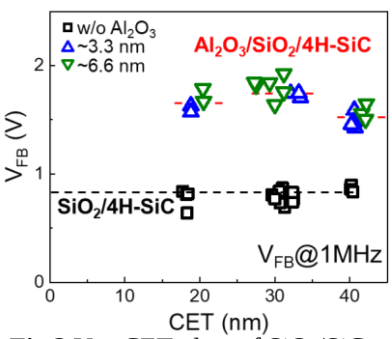

Fig.2 V_{FB}-CET plots of SiO_2/SiC MOS capacitors with and without Al_2O_3 thin film.

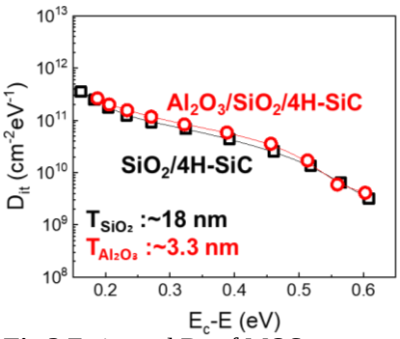

Fig.3 Estimated D_{it} of MOS capacitors with and without Al_2O_3 thin film by conductance method.