Top-gate monolayer MoS_2 MOSFETs with ZrO_2 gate dielectrics formed by low temperature ALD

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1. Introduction

MoS_2, a well-known TMDC channel material shows great potential in low-power-consumption device field. To fulfill the requirement of very-large-scale-integration (VLSI) applications, fabricating high performance top gate MoS_2 MOSFETs using chemical vapor deposition (CVD) grown MoS_2 with high quality gate dielectric is indispensable. Recently, we have reported uniform deposition of ZrO_2 on CVD-grown MoS_2 by plasma enhanced ALD (PEALD) [1]. Although high oxidation efficiency of PEALD promotes uniform layer deposition, the degradation of interfacial quality owing to MoS_2 oxidation was addressed.

In this study, uniform deposition of ZrO_2 as gate dielectrics on CVD-grown MoS_2 were obtained through ALD even at low deposition temperature at 150 °C, leading to significantly suppressed interfacial oxidation [2]. The device performance of top gate monolayer (1L) MoS_2 MOSFETs has also been demonstrated.

2. Experimental procedure

The detailed process flow for fabricating 1L MoS_2 top gate MOSFETs is shown Fig 1(a). The schematic cross-section and top view of optical microscope photograph of MoS_2 devices are shown in Fig. 1(b) and 1(c), respectively. Salt-assisted CVD was used to synthesize MoS_2 directly on SiO_2/Si substrates using MoO_2 and sulfur powder. KBr was used as a growth promoter, as described previously [3]. ZrO_2 gate dielectrics were deposited at 150 °C thorough ALD using TEMAZ and H_2O as precursors, which denotes as LT-ALD afterwards. MoS_2 samples deposited with PEALD ZrO_2 gate dielectrics at 300 °C [1] were also prepared for comparison, which denotes as HT-PEALD afterwards.

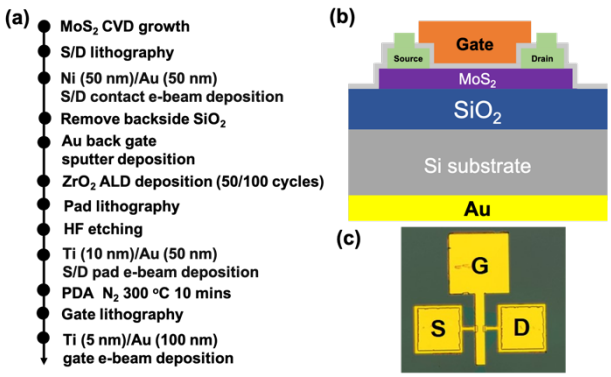

Fig. 1 (a) Process flow for fabricating MoS_2 top gate MOSFETs, (b) schematic cross-section and (c) top view of optical microscope photograph of the fabricated devices.

3. Results and discussion

Fig. 2 shows Mo 3d XPS spectra extracted from 2 nm thick ZrO_2 on bulk MoS_2, which was mechanically exfoliated from MoS_2 flakes. The spectrum extracted from pristine MoS_2 flakes is also shown for comparison. The Mo 3d spectra for pristine and LT-ALD samples show almost identical features with three distinct peaks, which are attributed to the MoS_2 states. This indicates that the ZrO_2 deposition on MoS_2 at 150 °C mainly results from physical absorption instead of chemical reaction between ZrO_2 and MoS_2. On the other hand, additional states corresponding to MoO_3 were observed in HT-PEALD samples, suggesting the formation of Mo oxide interfacial layer owing to high oxidation efficiency of HT PEALD. Fig. 3 shows the I_D-V_G characteristics of 5μm-gate-length 1L MoS_2 MOSFETs under top gate operation. Normal nMOSFETs operation behavior was clearly observed with a high on-off ratio of 10^7. Low subthreshold swing of ~90 mV/decade also indicates the benefit of suppressed interfacial oxidation, which leads to low damaged MoS_2 channel.

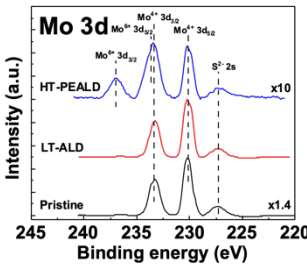

Fig. 2 Mo 3d XPS spectra extracted from HT-PEALD ZrO_2/MoS_2, LT-ALD ZrO_2/MoS_2 and pristine MoS_2, respectively

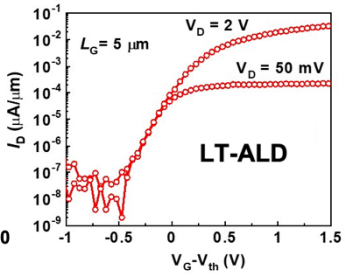

Fig. 3 I_D-V_G characteristics of 5μm-gate-length 1L MoS_2 MOSFETs under top gate operation

4. Conclusion

1L MoS_2 top gate MOSFETs using ALD ZrO_2 gate dielectrics has been demonstrated with VLSI-compatible gate stack formation processes. Low ALD deposition temperature promotes physical adsorption, leading to significantly suppressed surface oxidation and less damaged MoS_2 channel. low thermal budget process is beneficial for ultrathin MoS_2 channel.

Acknowledgment

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Reference

[1] W. H. Chang et al., *Silicon nano workshop* 91 (2019). [2] W. H. Chang et al., *JJAP* in press. [3] K. Kojima et al., *Nanoscale* 11, 12798 (2019).