Effect of Gate Voltage on the Thermoelectric Properties of an InGaZnO/SiO_2 Standard Thin Film Transistor

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Introduction

Indium gallium zinc oxide (InGaZnO) is commonly used as a channel layer thin film transistors (TFT) owing to its low temperature processability, superior mobility, and low leakage current [1]. However, its thermoelectric (TE) properties are relatively less-explored; most studies focused on pristine thin films [2]. In pristine InGaZnO thin films, there is a commonly observed maximum power factor (PF~0.07 mW/mK^2) owing to the coupled but opposing relationships of Seebeck coefficient (S) and electrical conductivity (σ) on the carrier concentration (n). In order to decouple these properties, the material structure is usually engineered such that the electron conduction is confined in an extremely narrow quantum well, such as in nanostructures of two-dimensional electron systems [3]. In this study, the TE performance of a typical InGaZnO TFT with SiO_2 gate insulator is investigated. In a typical TFT, electrons is expected to accumulate at the channel/insulator interface in its ON state, so it is expected to be a region of high σ. However, it has not been studied whether this region can also be thermoelectrically active.

Experimental

Bottom-gate top-contact TE-TFTs were fabricated on p-type Si gate electrode with 85 nm of thermally oxidized SiO_2 layer as the gate insulator. The InGaZnO channel (70 nm) was deposited via RF magnetron sputtering (In_2O_3:Ga_2O_3:ZnO = 2:2:1) at room temperature. The RF power and pressure during deposition were 100 W and 0.6 Pa, respectively. Next, a metal thin film layer (80 nm Ti/20 nm Au) was deposited via electron beam evaporation. The channel islands, as well as the source and drain electrodes were patterned by standard photolithography. Finally, the fabricated devices were post-annealed at 300°C for 2h under air (N_2:O_2 = 4:1). The transfer (I_D-V_G) and output (I_D-V_D) curves were obtained using a semiconductor parameter analyzer (Agilent 4156C). To measure the Seebeck coefficient (S), the method by Liang, et. al was adopted [4]. However, the ΔT was derived from thermal images obtained using an infrared thermal microscope (QFI) placed on top of the device. The power factor (PF=S^2σ) was then calculated using the electrical conductivity σ obtained from the I_D-V_D curves.

Results and Discussion

Fig. 1a reveals that the InGaZnO TE-TFT exhibit proper switching, with a μ = 10.4 cmV^{-1}S^{-1}. This suggests typical transistor behavior, even at a low V_D of 100 μV, where the Seebeck voltage is expected to range. Similarly, the PF exhibits a switching behavior under positive V_G, as revealed in Fig. 1b, with a maximum of ~0.1 mW/mK^2 at V_G = 40 V. This superior PF can mostly be attributed to the σ increasing by two orders of magnitude, while maintaining a decrease in S to only ~35%. This suggests a possible suppression of the coupling reaction of S and σ, owing to the electron confinement at the extremely narrow accumulation layer formed at the InGaZnO/SiO_2 interface. Using the Kamiya-Nomura percolation model, it was also determined that the TE-TFT can potentially reach about twice the predicted PF limit of pristine InGaZnO thin films. This suggests that an InGaZnO TFT can also simultaneously act as a TE device with a promising performance, which paves the way for future self-powered transparent electronic devices.

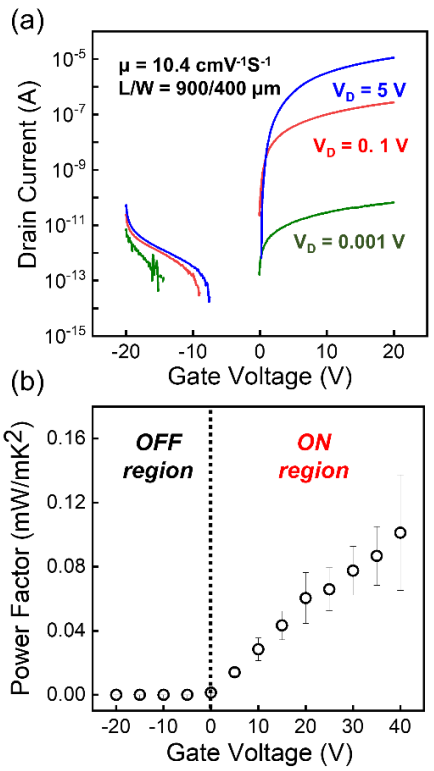

Fig. 1. (a) Transfer curve and (b) PF vs V_G plot of the InGaZnO/SiO_2 TE-TFT.

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